60 W 19 V SMPS demo board with ICE5GSAG and IPA80R650CE

DEMO_5GSAG_60W1

About this document

Scope and purpose

This document is an engineering report that describes a universal-input 60 W 19 V off-line flyback converter using the latest 5th generation Infineon Fixed Frequency Controller (FFC) ICE5GSAG and CoolMOS™ IPA80R650CE. It offers high-efficiency, low-standby power with selectable entry and exit standby power options, a wide V CC operating range with fast start-up, robust line protection with input Over Voltage Protection (OVP) and various modes of protection for a highly reliable system. This demo board is designed for users who wish to evaluate ICE5GSAG and IPA80R650CE in terms of optimized efficiency, thermal and EMI performance.

Intended audience

This document is intended for power-supply design/application engineers, students, etc., who wish to design low-cost and highly reliable systems of off-line SMPS, such as auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for blu-ray players, set-top boxes, games consoles, etc.

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1 Abstract

This is an engineering report for a 60 W 19 V demo board designed in a fixed frequency flyback converter topology using the fifth-generation FFC, ICE5GSAG, and a CE series of HV CoolMOS™, IPA80R650CE. The demo board is operated in Discontinuous Conduction Mode (DCM) and is running at 125 kHz fixed switching frequency. The frequency reduction with soft-gate driving and frequency jittering offers lower EMI and better efficiency from light loads up to 50% load. The selectable Active Burst Mode (ABM) power enables ultra-low power consumption. In addition, numerous adjustable protection functions have been implemented in ICE5GSAG to protect the system and customize the IC for the chosen application. In case of failure modes, like line over-voltage, V CC over-/under-voltage, open control-loop or over-load, over-temperature, V CC short-to-GND and CS short-to-GND, the device enters protection mode. By means of the cycle-by-cycle peak current Limitation (PCL), the dimensions of the transformer and the current rating of the secondary diode can both be optimized. Thus, a cost-effective solution can easily be achieved. The target applications of ICE5GSAG are either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

2 Demo board

This document contains the list of features, the power supply specifications, schematics, Bill of Materials (BOM) and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are shown at the end of the report.

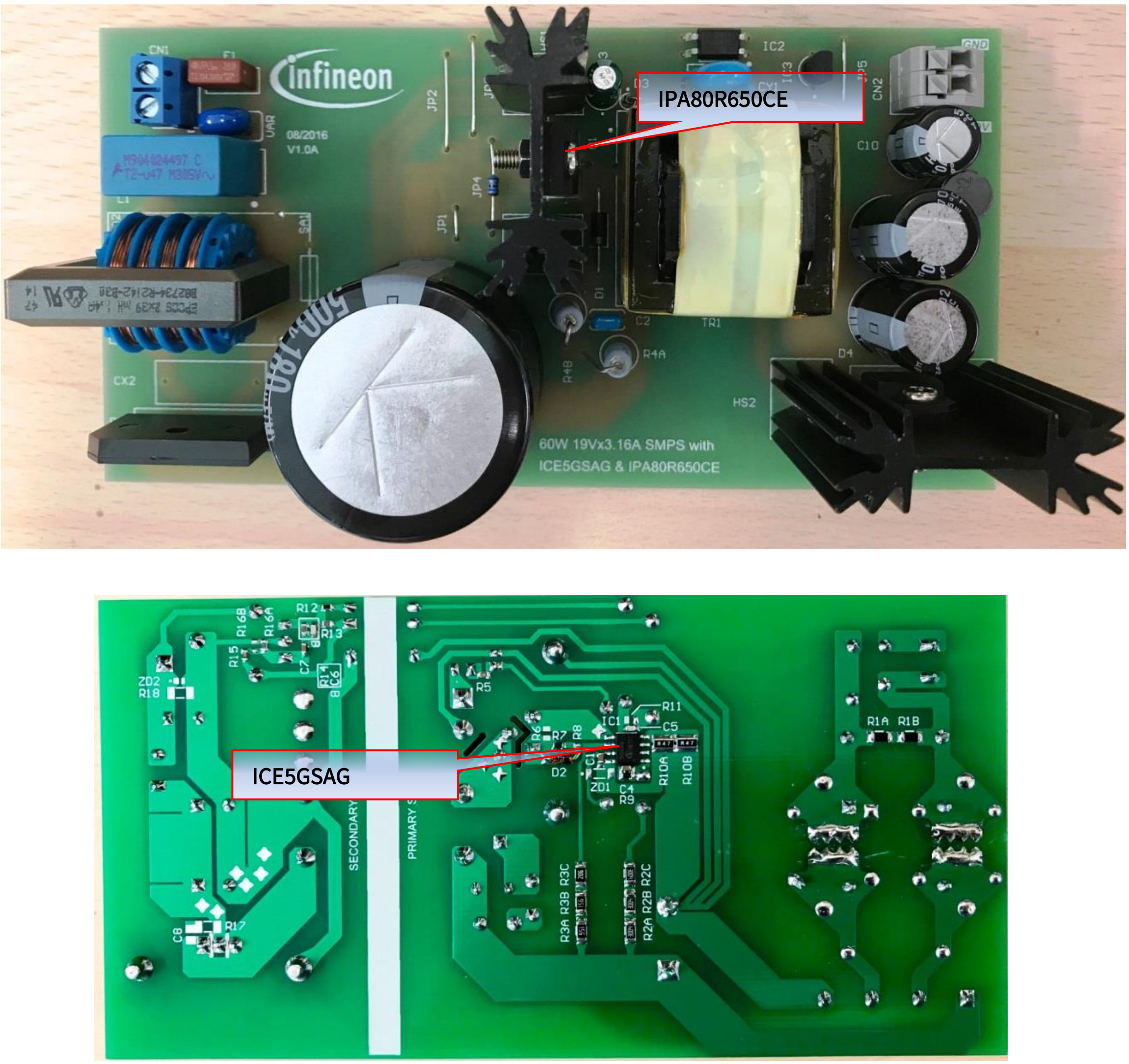


Figure 1 DEMO_5GSAG_60W1

3 Specifications of demo board

Table 1 Specifications of DEMO_5GSAG_60W1

Input voltage and frequency	85 V AC (60 Hz)~300 V AC (50 Hz)
Output voltage, current and power	19 V x 3.16 A = 60 W
Dynamic load response (load change from 10% to 100%, slew rate at 1.5 A/µs, 100 Hz)	±5% of nominal output voltage
Output ripple voltage (full-load, 85 V AC~300 V AC)	19 $V_{ripple\_p\_p}$ < 200 mV
Active mode four-point average efficiency (25%, 50%, 75%, 100% load)	> 86% at 115 V AC and 230 V AC
No-load power consumption	< 100 mW at 230 V AC
Conducted emissions (EN 55022 class B)	Pass with 7 dB margin for 115 V AC and 230 V AC
ESD immunity (EN 61000-4-2)	Special level (±10 kV for both contact and air discharge)
Surge immunity (EN 61000-4-5)	Installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth)
Form factor case size (L x W x H)	(144 x 73 x 43) mm^3

4 Circuit description

4.1 Line input

The AC-line input side comprises the input fuse F1 as over-current protection. The choke L1, X-capacitor CX1 and Y-capacitor CY1 act as EMI suppressors. Optional spark-gap devices SA1, SA2 and varistor VAR can absorb HV stress during a lightning surge test. A rectified DC voltage (120~424 V DC) is obtained through the bridge rectifier BR1 together with the bulk capacitor C3.

4.2 Start-up

To achieve fast and safe start-up, ICE5GSAG is implemented with start-up resistor and V CC short-to-GND protection. When V_{VCC} reaches the turn-on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5GSAG is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase in increments from 0.3 V to 1 V. After IC turn-on, the V CC voltage is supplied by auxiliary windings of the transformer. V CC short-to-GND protection is implemented during the start-up time.

4.3 PWM control with frequency reduction and switching MOSFET

The PWM pulse is generated by the 5th generation FFC ICE5GSAG. The new controller can be operated in either DCM or Continuous Conduction Mode (CCM) with frequency reduction mode to achieve the overall average efficiency. This demo board is designed to operate in DCM.

When the system is operating at maximum power, the controller will switch at the fixed frequency of 125 kHz. In order to achieve a better efficiency between light and medium loads, frequency reduction is implemented, and the reduction curve is shown in Figure 2. The V_{CS} is clamped by the current limitation threshold or by the PWM op amp while the switching frequency is reduced. After the maximum frequency reduction, the minimum switching frequency is f_{OSC2_MIN} (53 KHz).

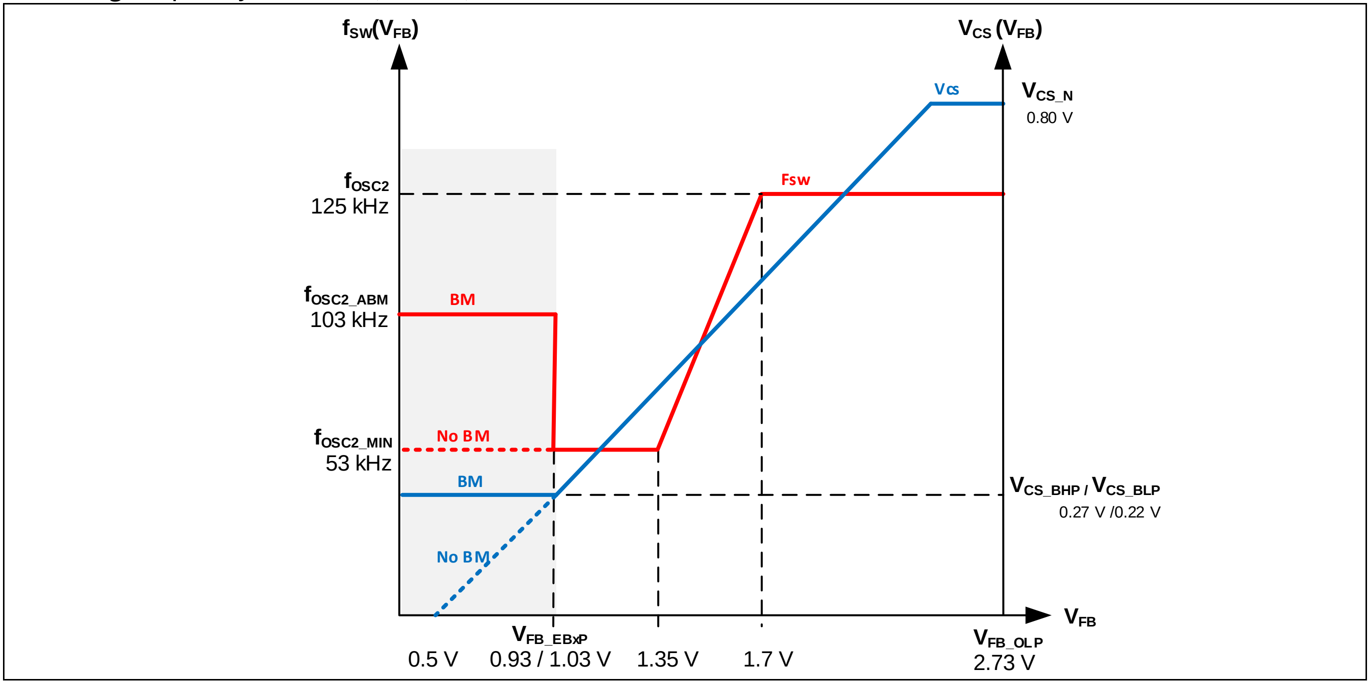


Figure 2 Frequency reduction curve

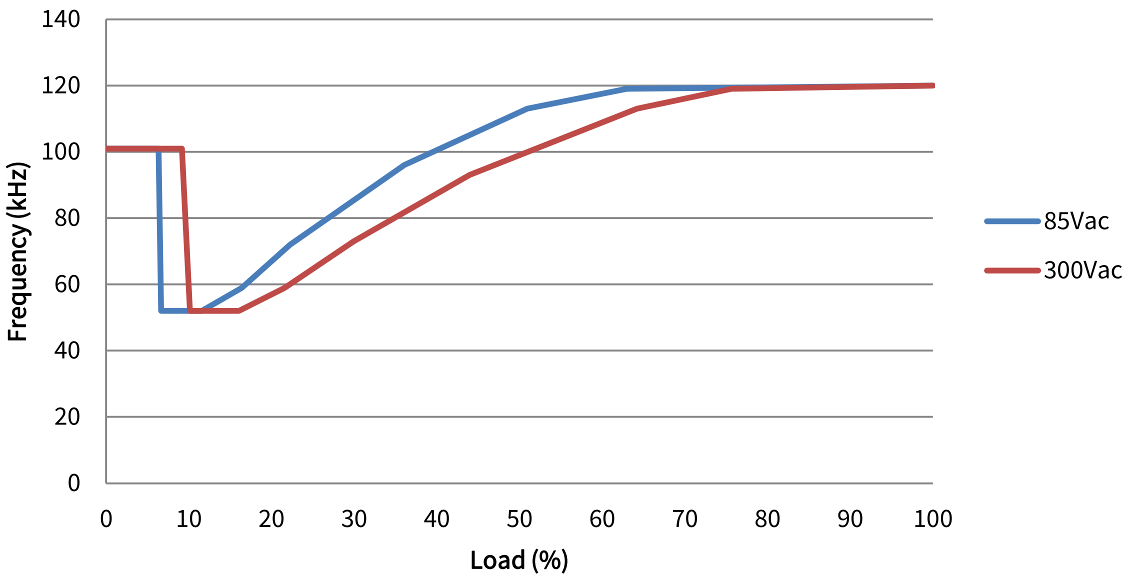


Figure 3 Frequency reduction curve of DEMO_5GSAG_60W1

The measured frequency reduction curve of DEMO_5GSAG60W1 is shown in Figure 3.
The PWM pulse drives the HV power MOSFET, IPA80R650CE. The CoolMOS™ provides all the benefits of a fast-switching superjunction (SJ) MOSFET while not sacrificing ease of use. It achieves extremely low conduction and switching losses, and can make switching applications more efficient, more compact, lighter and cooler. Details about the information mentioned above are illustrated in the product datasheet.

4.4 Frequency jittering

The ICE5GSAG has a frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 125 kHz (±5 kHz) and the jitter period is 4 ms.

4.5 RCD clamper circuit

A clamper network (R4A, R4B, C2 and D1) dissipates the energy of the leakage inductance and suppresses ringing on the SMPS transformer.

4.6 Output stage

On the secondary side the power is coupled out by Schottky diode D4. The capacitors C9A and C9B provide energy buffering, following with the LC filters L2 and C10 to reduce the output voltage ripple considerably. Storage capacitors C9A and C9B are selected to have a very small internal resistance (ESR) to minimize the output voltage ripple.

4.7 Feedback loop

For feedback (FB), the output is sensed by the voltage divider of R15, R16A and R16B and compared to the IC3 (TL431) internal reference voltage. C7, C6 and R14 comprise the compensation network. The output voltage of IC3 (TL431) is converted to the current signal via optocoupler IC2 and two resistors, R12 and R13, for regulation control.

4.8 Active Burst Mode (ABM)

ABM entry and exit power can be selected from three options, including no ABM. This demo board is set to level 3, and details are shown in the product datasheet. Under light load conditions, the SMPS enters ABM. At this stage, the controller is always active but the V_{VCC} must be kept above the switch-off threshold. During ABM, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load-jump.

For determination of entering ABM operation, two conditions apply:

1. The FB voltage is lower than the threshold of V_{FB_EBXP}, and
2. A certain blanking time (t_{FB_BEB}=36 ms) is required

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low during the preset blanking time.

During ABM, switching frequency is reduced to 103 kHz for level 2 and 3 selections and 53 kHz for level 1 (no ABM) to improve the efficiency during standby power measurement. The maximum Current Sense (CS) voltage is reduced from V_{CS_N} to V_{CS_BXP} to reduce the conduction loss and the audible noise. In ABM, the FB voltage changes like a sawtooth between $V_{FB\_Bon\_ISO}$ and $V_{FB\_Boff\_ISO}$.

The FB voltage immediately increases if there is a high load-jump. This is observed by one comparator. As the current limit is 27/33% during ABM a certain load is needed so that FB voltage can exceed V_{FB_LB} (2.75 V). After leaving ABM, maximum current can now be provided to stabilize V_{out}.

5 Protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5GSAG provides comprehensive protection to ensure the system is operating safely. This includes line over-voltage, V CC over-voltage and under-voltage, over-load, over-temperature (controller junction), CS short-to-GND and V CC short-to-GND. When those faults are found, the system will go into protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions are shown in the table below.

Table 2 Protection functions of ICE5GSAG

Protection function	Failure condition	Protection mode
Line over-voltage	V_{VIN} > 2.9 V	Non-switch auto restart
V CC over-voltage	V_{VCC} > 25.5 V	Odd-skip auto restart
V CC under-voltage	V_{VCC} < 10 V	Auto restart
Over-load	V_{FB} > 2.75 V and lasts for 54 ms	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J > 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} < 0.1 V and lasts for 0.4 µs and 3 consecutive pulses	Odd-skip auto restart
V CC short-to-GND (V_{VCC} = 0 V, $R_{Start-up}$ = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} < 1.2 V, $I_{VCC\_Charge1}$ ≈ -0.27 mA	Cannot start up

6 Circuit diagram

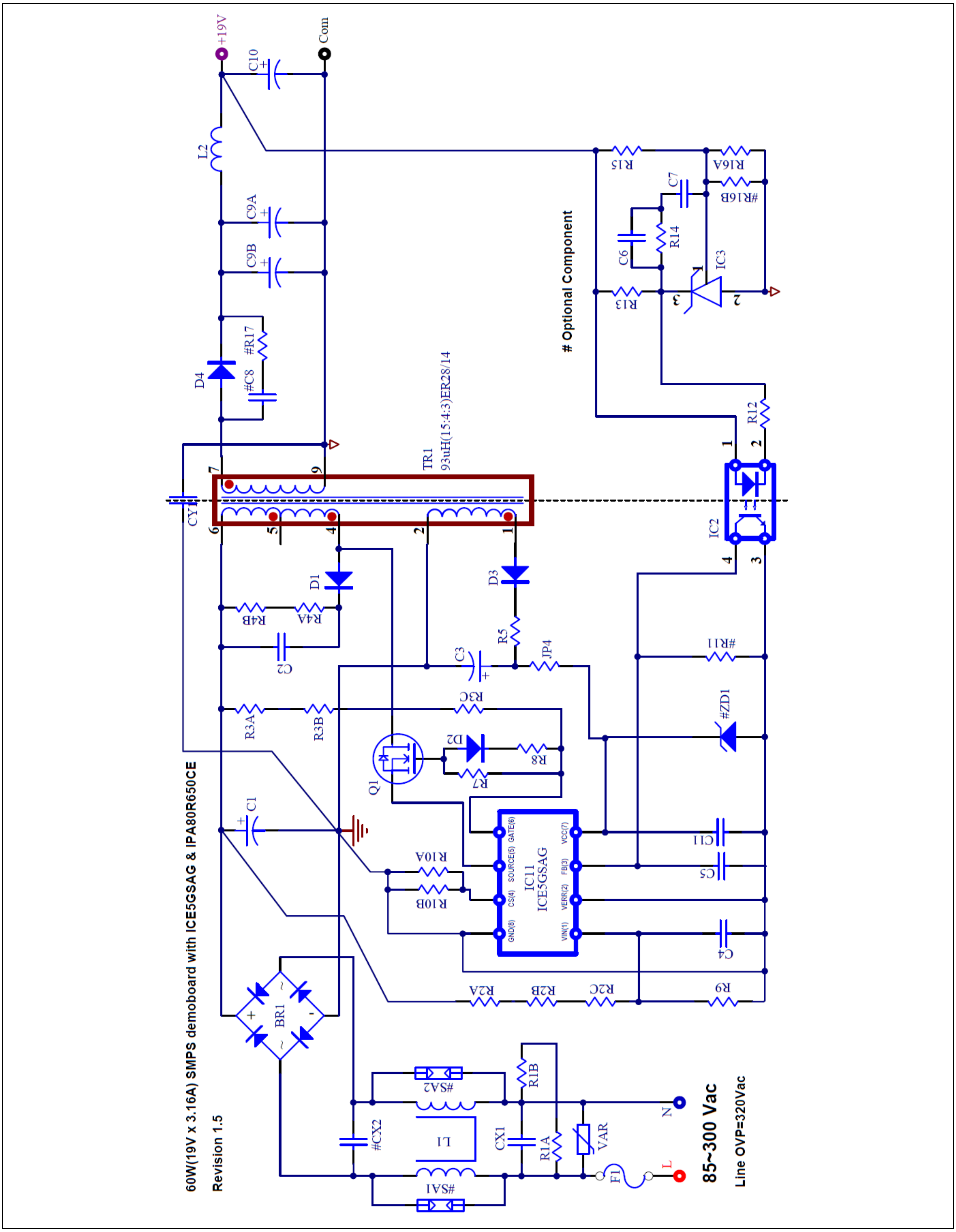


Figure 4 Schematic of DEMO_5GSAG_60W1

7 PCB layout

7.1 Top side

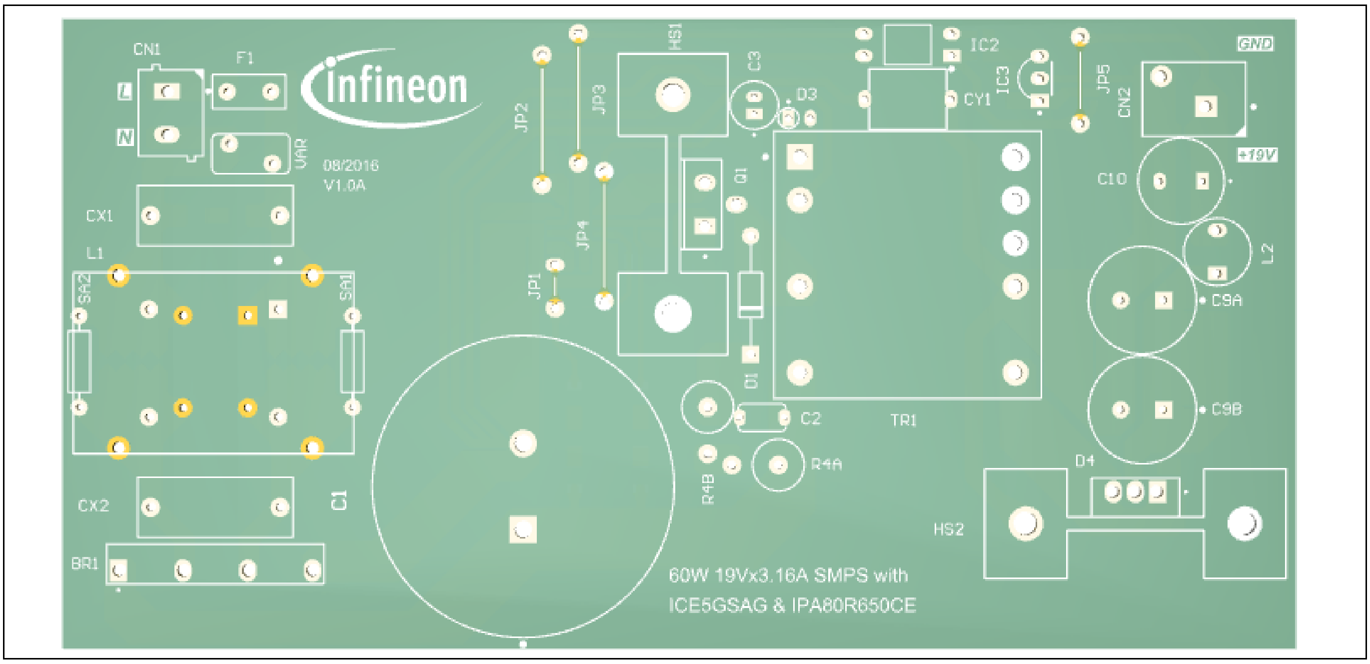


Figure 5 Top side component legend

7.2 Bottom side

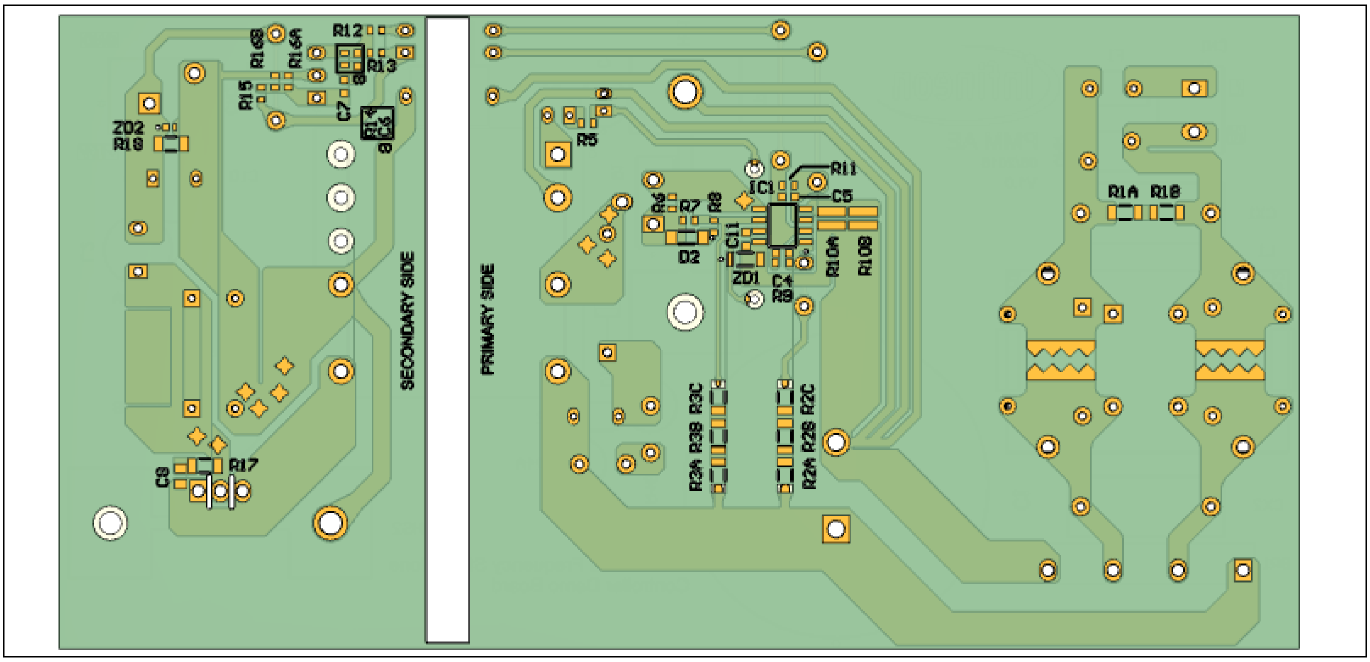


Figure 6 Bottom side copper and component legend

8 BOM

Table 3 BOM (R 1.5)

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/4 A	D4SB60L	Shindengen	1
2	CX1	0.47 µF/305 V	B32922C3474	Epcos	1
3	CY1	2.2 nF/500 V	DE1E3RA222MA4BQ	Murata	1
4	C1	180 µF/500 V	500VXG180MEFCSN35X30	Rubycon	1
5	C2	1 nF/1000 V	RDE7U3A102J2K1H03	Murata	1
6	C3	33 µF/50 V	35PX33MEFC5X11	Rubycon	1
7	C11	100 nF/50 V	GRM188R71H104KA93D	Murata	1
8	C5, C6	1 nF/50 V	GRM1885C1H102GA01D	Murata	2
9	C4	22 nF/50 V	GCM188R71H223KA37D	Murata	1
10	C9A, C9B	1500 uF/25 V	25ZLS1500MEFC12.5X20	Rubycon	2
11	C10	470 uF/25 V	25ZLH470MEFC10X12.5	Rubycon	1
12	C7	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
13	D1	1 A/800 V	UF4006		1
14	D2	0.2 A/150 V/50 ns	FDH400		1
15	D3	0.5 A/200 V	1N485B		1
16	D4	30 A/200 V	VF30200C		1
17	F1	3.15 A/300 V	36913150000		1
18	HS1, HS2	Heatsink	513102B02500G		2
19	IC1	ICE5GSAG	ICE5GSAG	Infineon	1
20	IC2	Optocoupler	SFH617A-3		1
21	IC3	Shunt regulator	TL431BVLPG		1
22	JP1, JP2, JP3, JP5	Jumper			4
23	L1	39 mH/1.4 A	B82734R2142B030	Epcos	1
24	L2	2.2 uH/6 A	744772022	Wurth Electronics	1
25	Q1	800 V/650 mΩ	IPA80R650CE	Infineon	1
26	R4A, R4B	15 kR/2 W/350 V	ERG-2SJ153		2
27	JP4	27 Ω			1
28	R5, R8	0 Ω (0603)			2
29	R10A, R10B	0.47 R/0.75 W/±1%	ERJ-B2BFR47V		2
30	R3A, R3B	15 MR/0.25 W/5%	RC1206JR-0715ML		2
31	R3C	20 MR/0.25 W/5%	RC1206JR-0720ML		1
32	R2A, R2B, R2C	3 MR/0.25 W/1%	RC1206FR-073ML		3
33	R9	59 kR/0.1 W/0.5%	ERJ-3RBD5902V		1
34	R1A, R1B	1 MΩ/5%/200 V	RC1206JR-071ML		2
35	R7	15 Ω (0603)			1
36	R12	1.5 kΩ (0603)			1
37	R13	1.2 kΩ (0603)			1
38	R14	22 kΩ (0603)			1
39	R15	66 kΩ (0603)			1

40	R16A	10 kΩ (0603)			1
41	TR1	93 µH (15:4:3) ER28/14	750343380 (Rev 0.4)	Wurth Electronics	1
42	VAR	0.25 W/320 V	B72207S2321K101	Epcos	1
43	Con (L N)	Connector	691102710002	Wurth Electronics	1
44	Con (+19 V com)	Connector	691 412 120 002B	Wurth Electronics	1

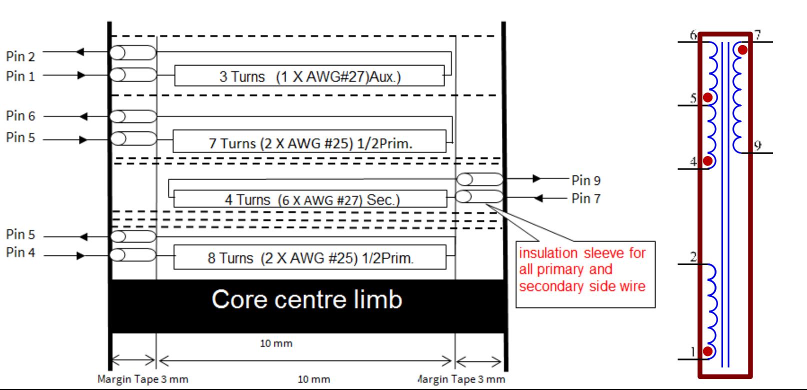
9 Transformer construction

Core and materials: ER28/14, TP4A (TDG)

Bobbin: 070-4869 (12-pin, THT, horizontal version)

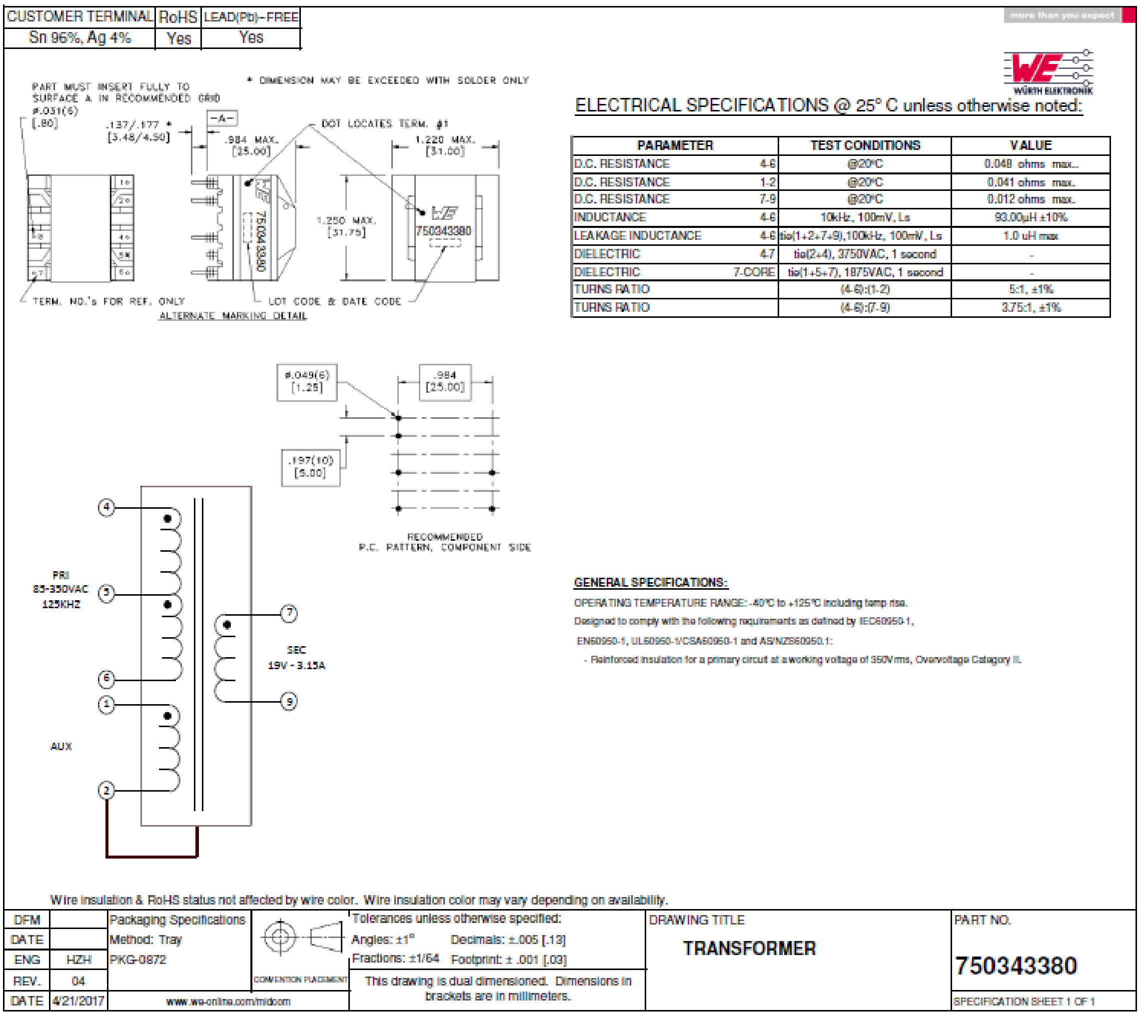
Primary inductance: Lp = 93 µH (±10%), measured between pin 4 and pin 6

Manufacturer and part number: Wurth Electronics Midcom (750343080 R04)



Start	Stop	Turns	Wire size	Layer
4	5	8	2 X AWG#25	1/2 Primary
7	9	4	6 X AWG#27	Secondary
5	6	7	2 X AWG#25	1/2 Primary
1	2	3	1XAWG#27	Auxiliary

Horizontal and vertical external shields are added and tied to pin 2



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	4-6	@20°C	0.048 ohms max..
D.C. RESISTANCE	1-2	@20°C	0.041 ohms max.
D.C. RESISTANCE	7-9	@20°C	0.012 ohms max.
INDUCTANCE	4-6	10kHz, 100mV, Ls	93.00µH ±10%
LEAKAGE INDUCTANCE	4-6	tie(1+2+7+9),100kHz, 100mV, Ls	1.0 uH max
DIELECTRIC	4-7	tie(2+4), 3750VAC, 1 second	-
DIELECTRIC	7-CORE	tie(1+5+7), 1875VAC, 1 second	-
TURNS RATIO		(4-6):(1-2)	5:1, ±1%
TURNS RATIO		(4-6):(7-9)	3.75:1, ±1%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:

- Reinforced insulation for a primary circuit at a working voltage of 350Vrms, Overvoltage Category II.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	Tolerances unless otherwise specified:	DRAWING TITLE
DATE		Method: Tray	Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER
ENG	HZH	PKG-0872	Fractions: ±1/64 Footprint: ± .001 [.03]	PART NO. 750343380
REV.	04	CONVENTION PLACEMENT	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	
DATE	4/21/2017	www.we-online.com/midcom		SPECIFICATION SHEET 1 OF 1

Figure 7 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	V_{out} (V DC)	I_{out} (A)	V_{RPP} (mV)	P_{out} (W)	Efficiency η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85 V AC/60 Hz	0.05670	19.05	0.000	115				81.00	3.51
	17.47	19.05	0.793	32	15.10	86.42	85.30		
	35.01	19.05	1.581	58	30.12	86.04			
	53.06	19.05	2.370	70	45.15	85.09			
	71.95	19.05	3.160	97	60.20	83.67			
115 V AC/60 Hz	0.06249	19.05	0.000	118				80.60	3.60
	17.32	19.05	0.793	44	15.10	87.17	86.85		
	34.49	19.05	1.581	58	30.12	87.34			
	51.90	19.05	2.370	76	45.15	86.99			
	70.06	19.05	3.160	90	60.20	85.92			
230 V AC/50 Hz	0.09808	19.05	0.000	113				82.00	3.79
	17.45	19.05	0.793	36	15.10	86.52	87.41		
	34.40	19.05	1.581	43	30.12	87.56			
	51.36	19.05	2.370	63	45.15	87.91			
	68.68	19.05	3.160	86	60.20	87.65			
265 V AC/50 Hz	0.11717	19.05	0.000	121				86.00	3.94
	17.59	19.05	0.793	33	15.10	85.83	87.02		
	34.59	19.05	1.581	40	30.12	87.08			
	51.50	19.05	2.370	55	45.15	87.67			
	68.80	19.05	3.160	78	60.20	87.50			
300 V AC/50 Hz	0.14020	19.05	0.000	123				89.00	4.00
	17.73	19.05	0.793	36	15.10	85.15	86.39		
	34.91	19.05	1.581	40	30.12	86.28			
	51.90	19.05	2.370	50	45.15	86.99			
	69.08	19.05	3.160	70	60.20	87.14			

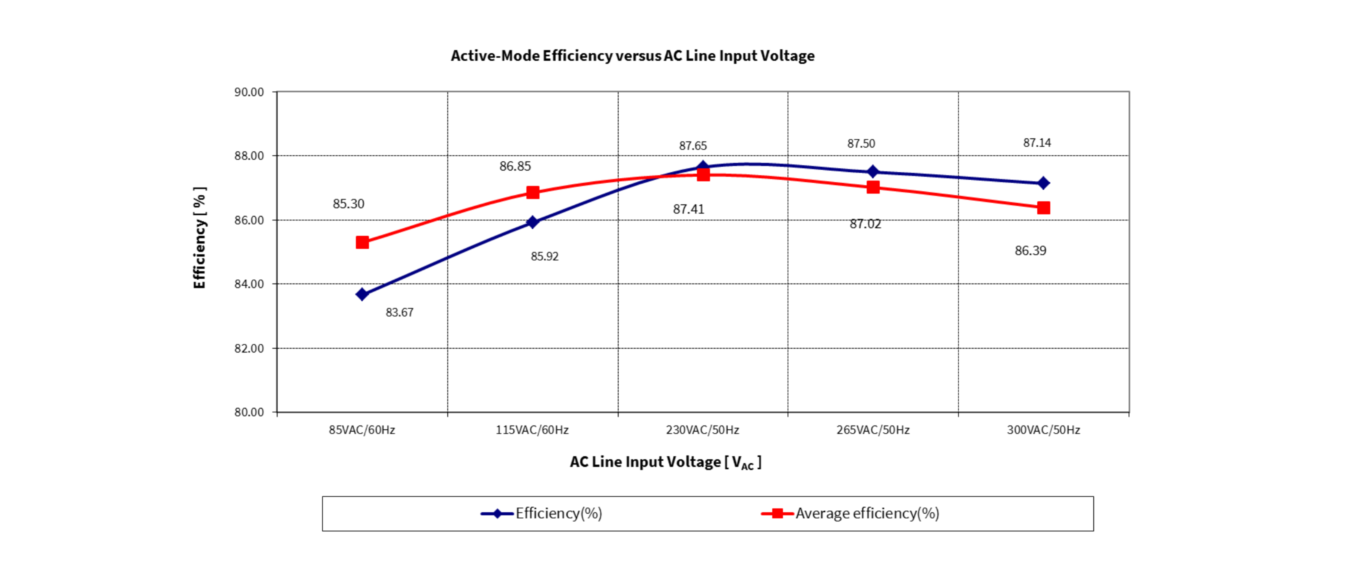


Figure 8 Efficiency vs AC-line input voltage

10.2 Standby power

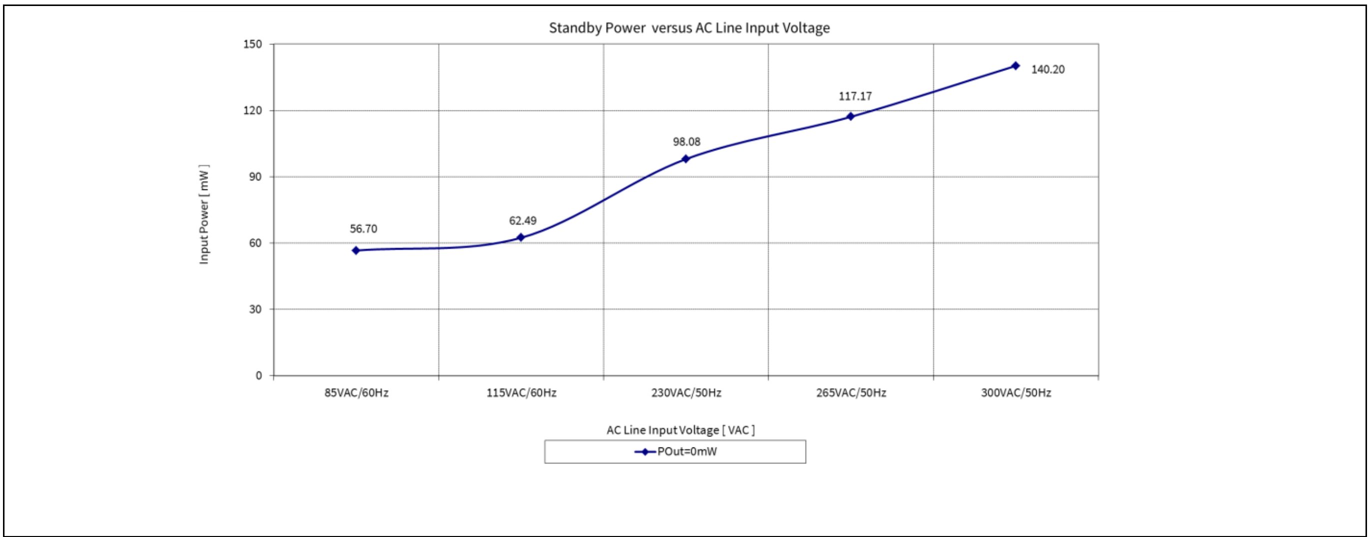


Figure 9 Standby power at no-load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

10.3 Line regulation

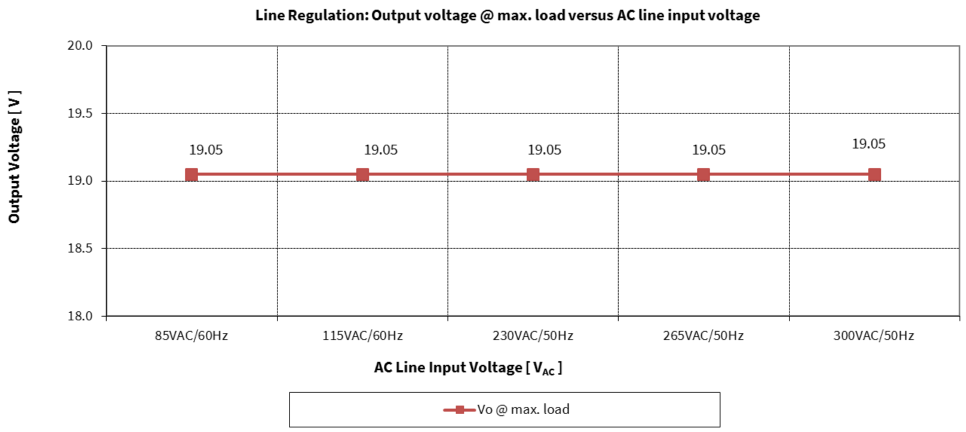


Figure 10 Line regulation V_{Out} at full-load vs AC-line input voltage

10.4 Load regulation

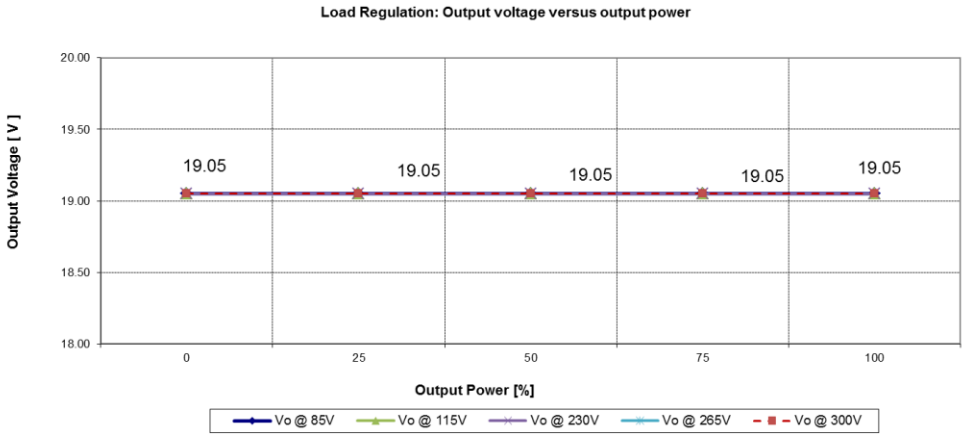


Figure 11 Load regulation V_{Out} vs output power

10.5 Maximum input power

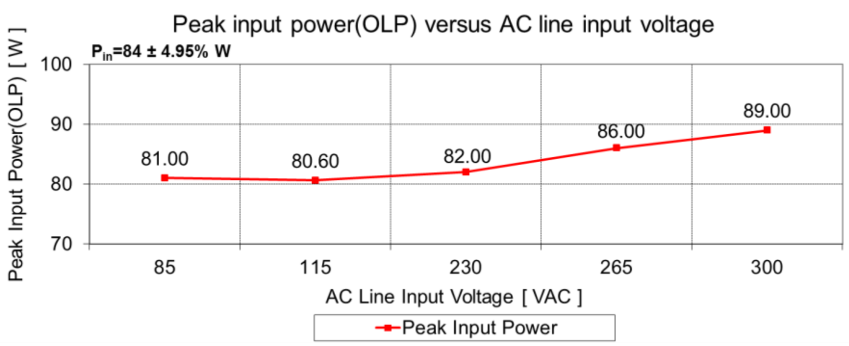


Figure 12 Maximum input power (before over-load protection) vs AC-line input voltage

10.6 ESD immunity (EN 61000-4-2)

Pass EN 61000-4-2 special level (±10 kV for both contact and air discharge).

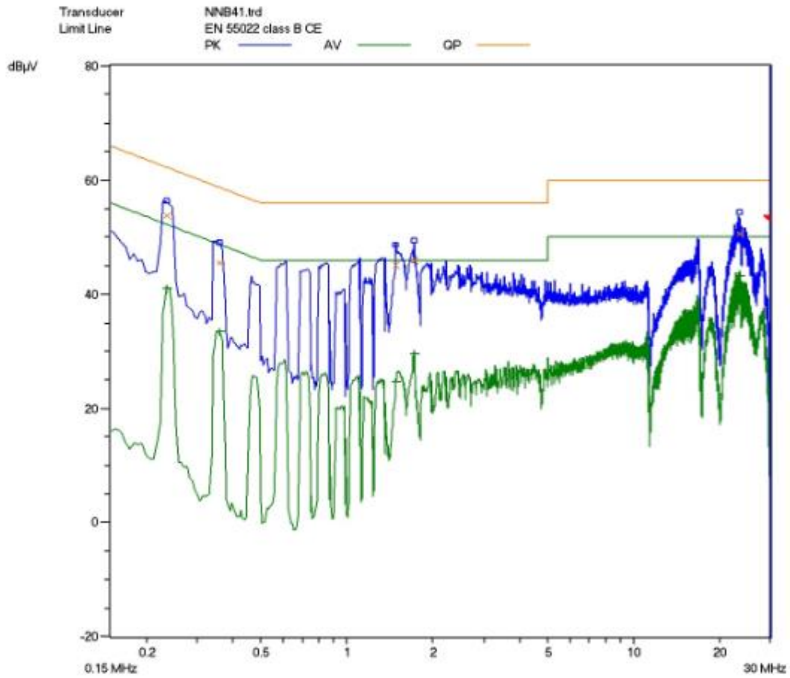
10.7 Surge immunity (EN 61000-4-5)

Pass EN 61000-4-5 installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth).[1]

10.8 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The demo board was set up at maximum load (60 W) with input voltage of 115 V AC and 230 V AC.

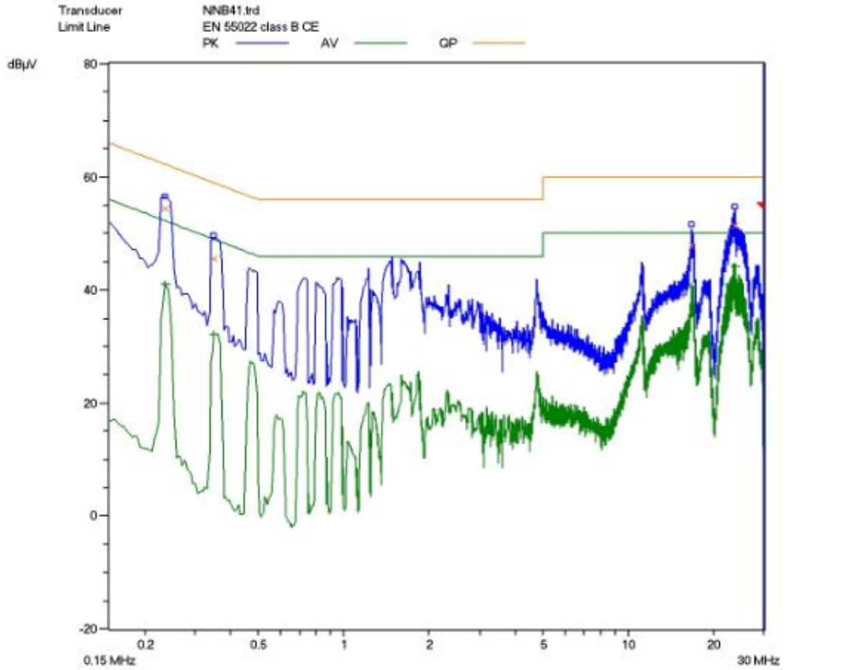
Pass conducted emissions EN 55022 (CISPR 22) class B with 7 dB margin for quasi peak measurement at low-line (115 V AC) and high-line (230 V AC).



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2340	L	56.5	L	41.0	L	53.9	52.3	62.3
0.3600	L	49.1	L	33.5	L	45.6	48.7	58.7
1.4820	L	48.7	L	24.7	L	45.1	46.0	56.0
1.7160	L	49.5	L	29.6	L	45.9	46.0	56.0
23.5440	L	54.4	L	43.2	L	50.6	50.0	60.0

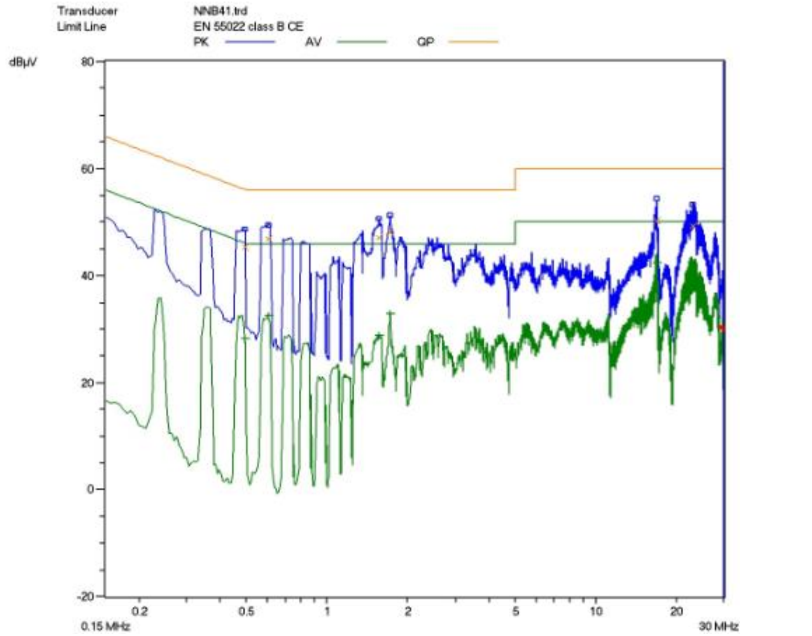
Figure 13 Conducted emissions (line) at 115 V AC and maximum load

[1] PCB spark-gap distance needs to reduce to 0.5 mm.



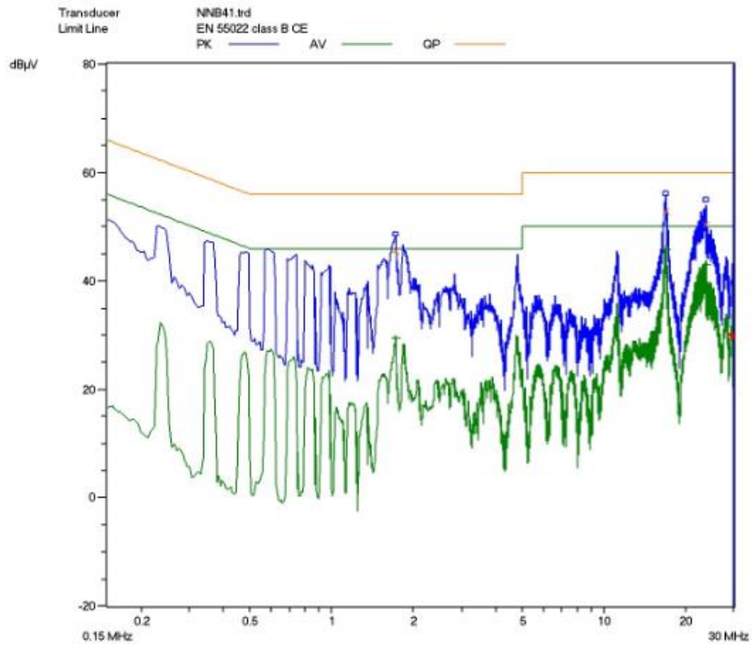
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2340	N	56.6	N	41.0	N	54.4	52.3	62.3
0.3480	N	49.6	N	32.2	N	45.6	49.0	59.0
16.7840	N	51.6	N	40.6	N	48.0	50.0	60.0
23.6640	N	54.8	N	44.1	N	51.5	50.0	60.0

Figure 14 Conducted emissions (neutral) at 115 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4920	L	48.7	L	28.2	L	45.4	46.1	56.1
0.6060	L	49.5	L	32.5	L	47.0	46.0	56.0
1.5660	L	50.7	L	28.8	L	47.2	46.0	56.0
1.7160	L	51.3	L	32.9	L	48.0	46.0	56.0
16.8000	L	54.3	L	42.3	L	50.3	50.0	60.0
23.1040	L	53.2	L	41.6	L	49.2	50.0	60.0

Figure 15 Conducted emissions (line) at 230 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
1.7160	N	48.8	N	29.4	N	45.6	46.0	56.0
16.8400	N	56.2	N	45.7	N	52.9	50.0	60.0
23.6400	N	55.0	N	43.0	N	50.5	50.0	60.0

Figure 16 Conducted emissions (neutral) at 230 V AC and maximum load

10.9 Thermal measurement

The thermal test of the open-frame demo board was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements were taken after one hour running at full-load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC11 (ICE5GSAG)	85.5	56.2
2	Q11 (IPA80R650CE)	58.9	60.5
3	R14A (CS resistor)	79.0	48.2
4	TR1 (transformer)	70.4	82.0
5	BR1 (bridge diode)	63.3	38.0
6	R11A (clamper resistor)	54.8	55.0
7	L11 (choke)	85.0	42.0
8	D21 (secondary diode)	61.8	60.6
9	Ambient	25.0	25.0

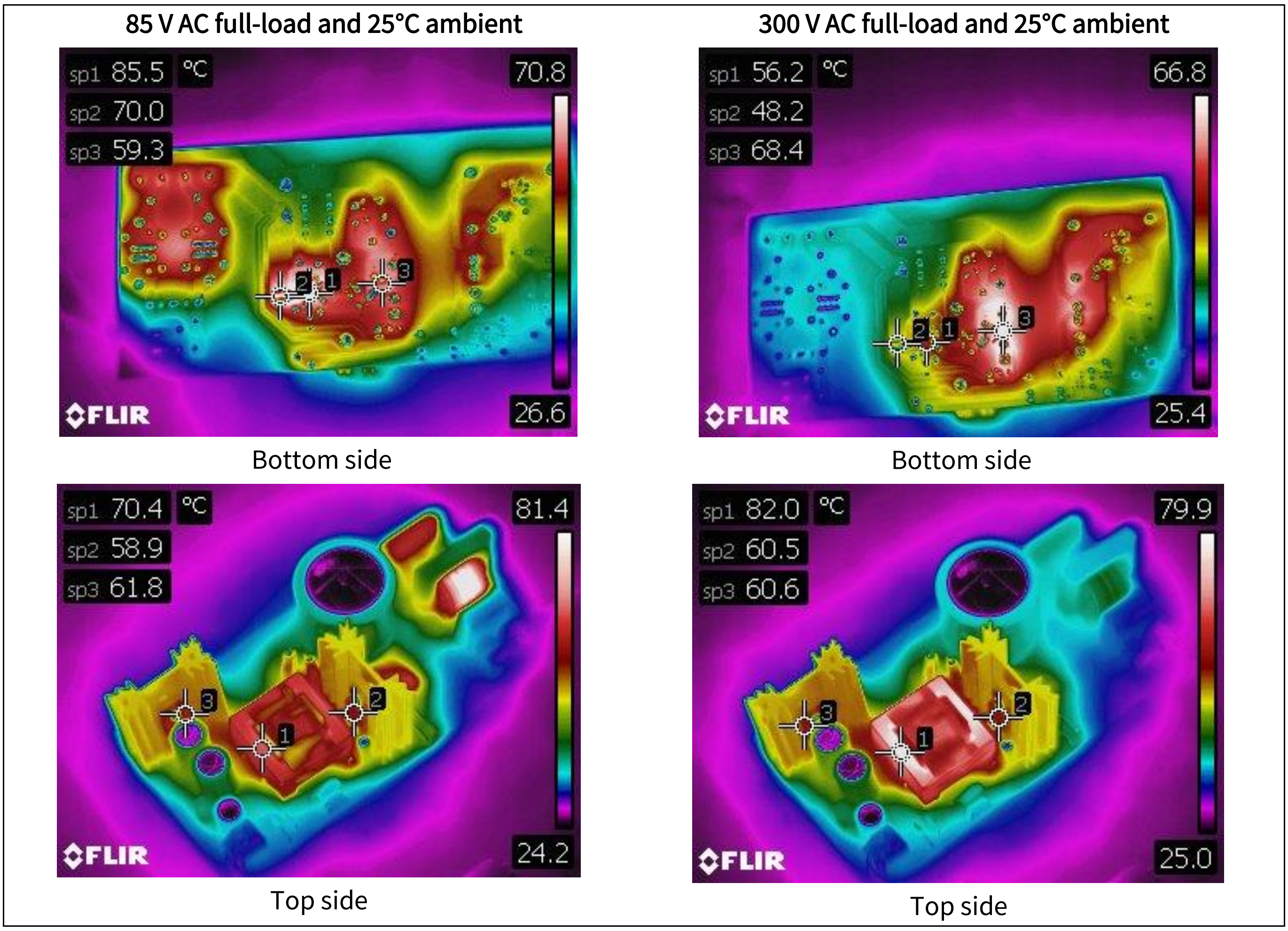


Figure 17 **Infrared thermal image of DEMO_5GSAG_60W1**

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

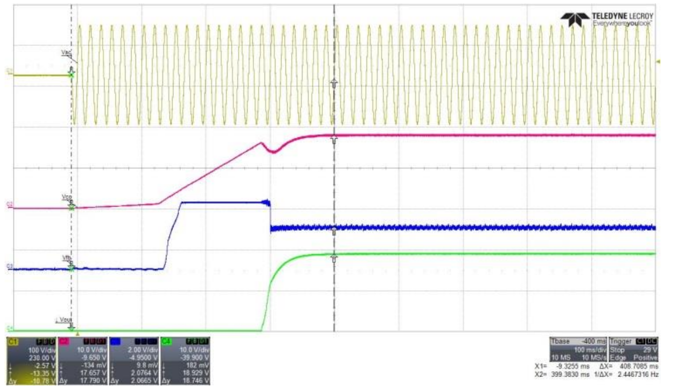
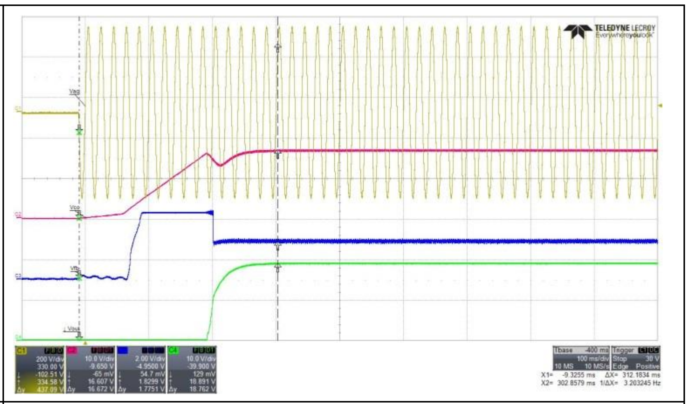
	
C1 (yellow) : AC-line voltage (V AC) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : 19 V output voltage (V_{Out})	C1 (yellow) : AC-line voltage (V AC) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : 19 V output voltage (V_{Out})
Start-up time at 85 V AC and maximum load ≈ 408 ms	Start-up time at 300 V AC and maximum load ≈ 312 ms

Figure 18 Start-up

11.2 Soft-start

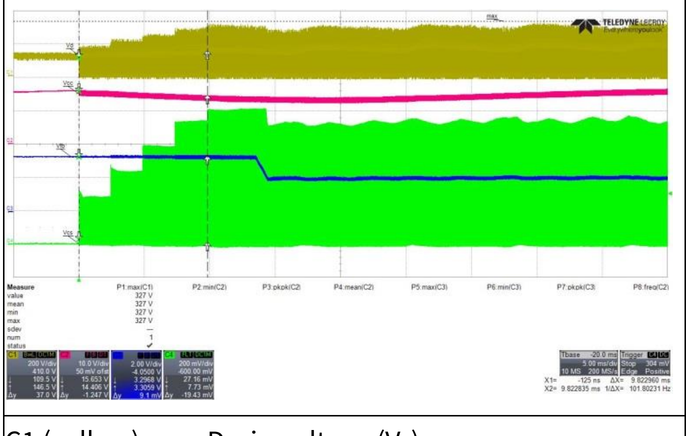
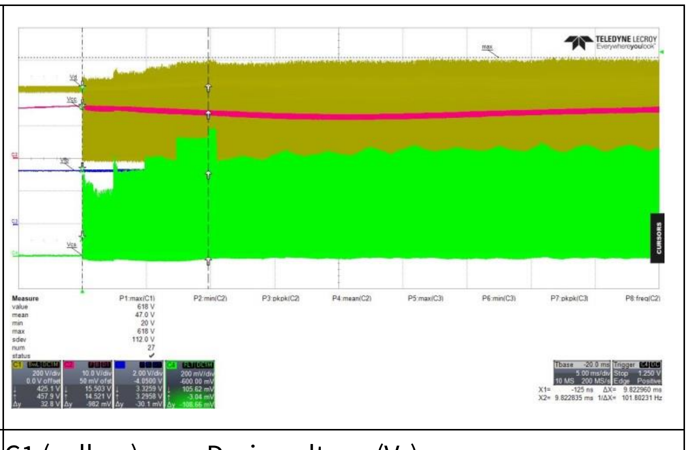
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Soft-start time at 85 V AC and maximum load ≈ 10 ms	Soft-start time at 300 V AC and maximum load ≈ 10 ms

Figure 19 Soft-start

11.3 Drain and CS voltage at maximum load

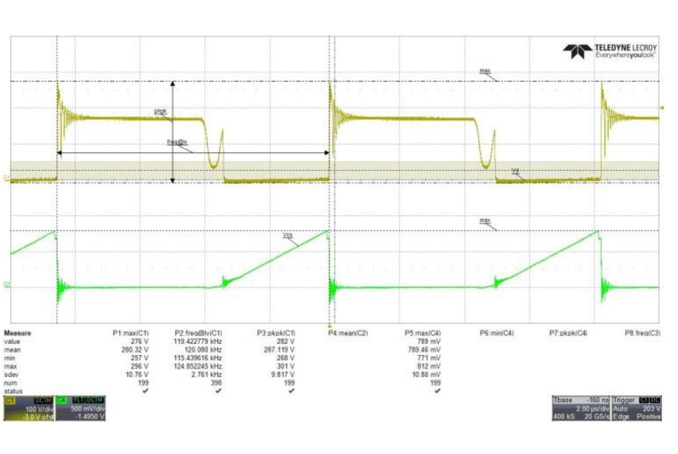
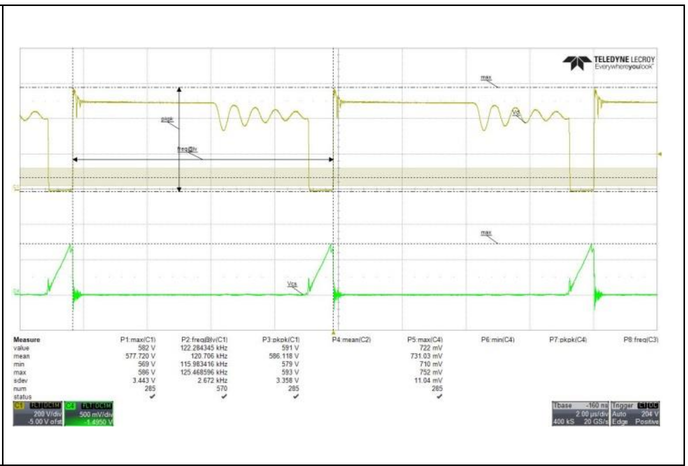
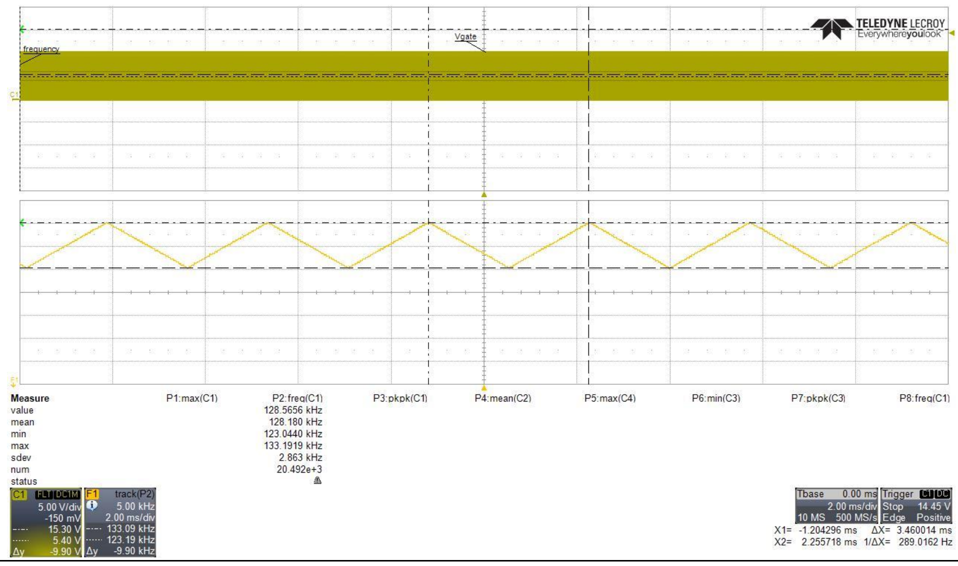
	
C1 (yellow) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
V_{Drain_peak} at 85 V AC ≈ 301 V	V_{Drain_peak} at 300 V AC ≈ 593 V

Figure 20 Drain and CS voltage at maximum load

11.4 Frequency jittering



C1 (yellow) : Gate voltage (V_G)

F1 (yellow) : Frequency track of gate (V_{GATE})

Frequency jittering at 85 V AC and maximum load ≈ 123 kHz~128 kHz, jitter period ≈ 3.4 ms

Figure 21 Frequency jittering

11.5 Load transient response (dynamic load from 10% to 100%)

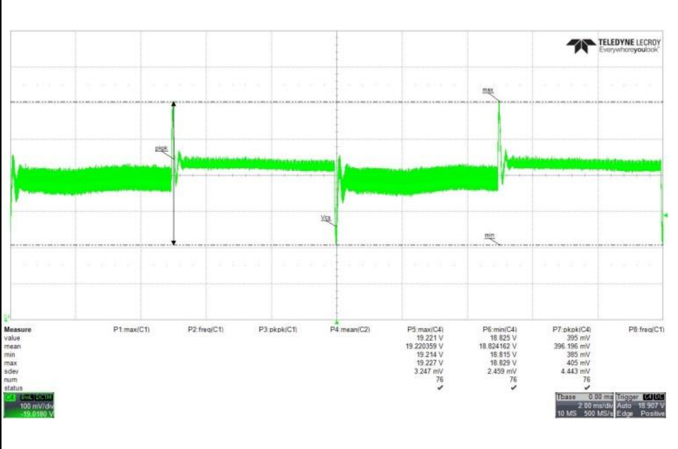
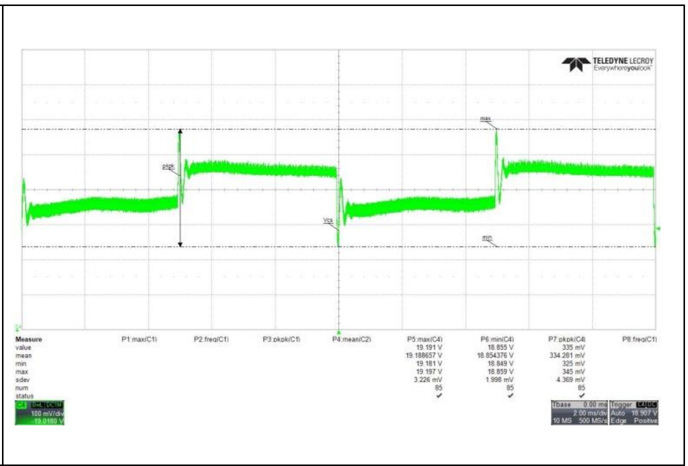
	
C4 (green) : 19 V output ripple voltage (V_{Out})	C4 (green) : 19 V output ripple voltage (V_{Out})
19 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 405 mV (85 V AC, load change from 10% to 100%, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	19 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 345 mV (300 V AC, load change from 10% to 100%, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 22 Load transient response

11.6 Output ripple voltage at maximum load

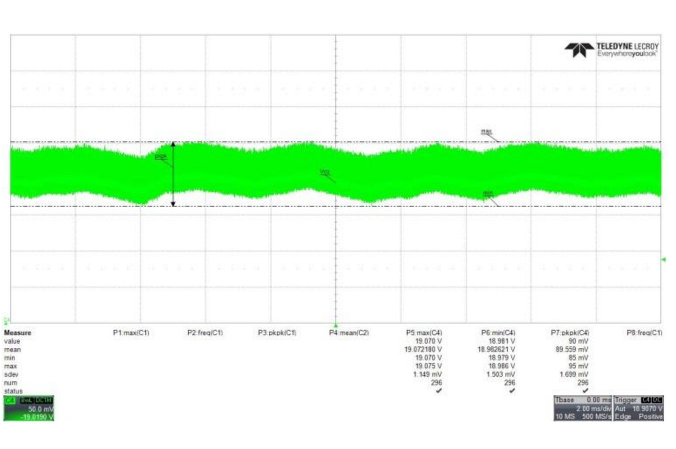
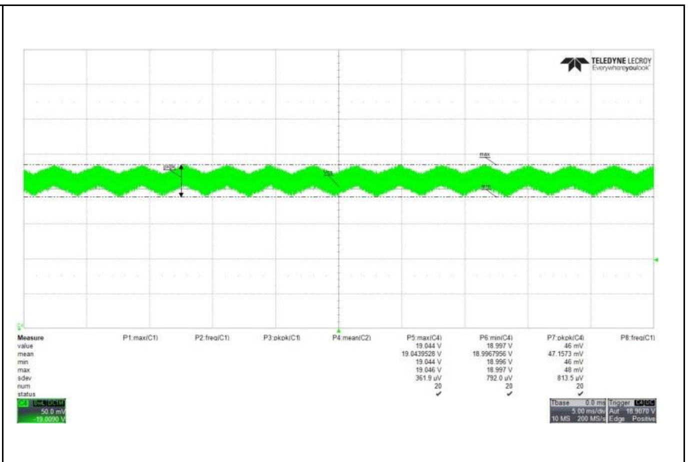
	
C4 (green) : 19 V output ripple voltage (V_{Out})	C4 (green) : 19 V output ripple voltage (V_{Out})
19 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 97 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	19 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 70 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 23 Output ripple voltage at maximum load

11.7 Output ripple voltage at ABM 1 W load

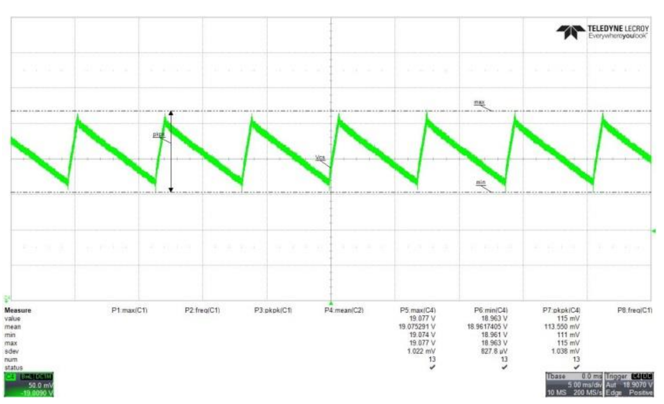
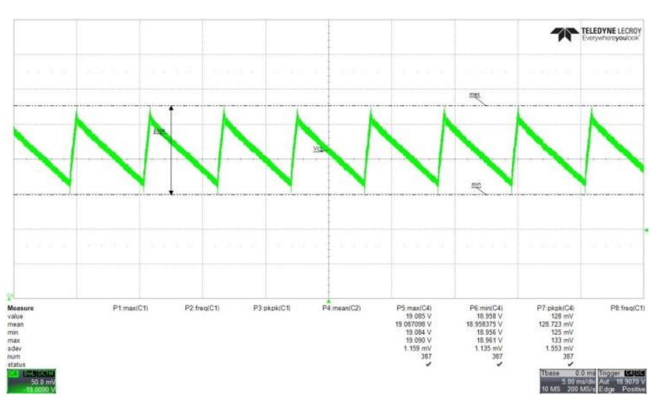
	
C4 (green) : 19 V output ripple voltage (V_{Out})	C4 (green) : 19 V output ripple voltage (V_{Out})
19 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 115 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	19 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 133 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 24 Output ripple voltage at burst mode 1 W load

11.8 Entering ABM

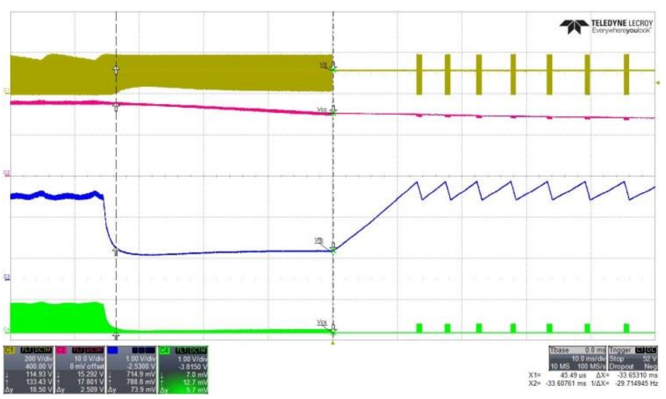
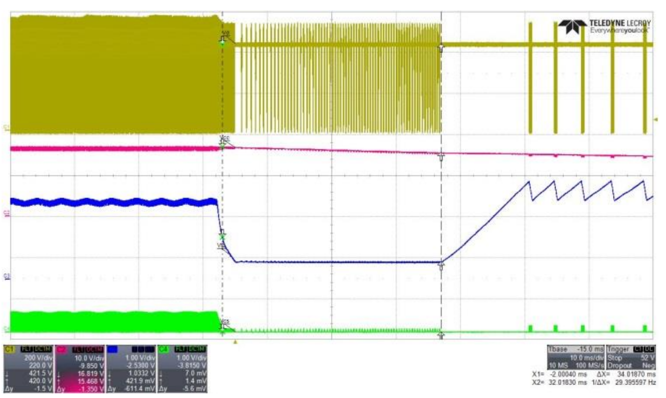
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to enter ABM level 1: V_{FB} < 1.05 V and $t_{blanking}$ = 36 ms (load change from full-load to 1 W load at 85 V AC)	Condition to enter ABM level 1: V_{FB} < 1.05 V and $t_{blanking}$ = 36 ms (load change from full-load to 1 W load at 300 V AC)

Figure 25 Entering ABM

11.9 During ABM

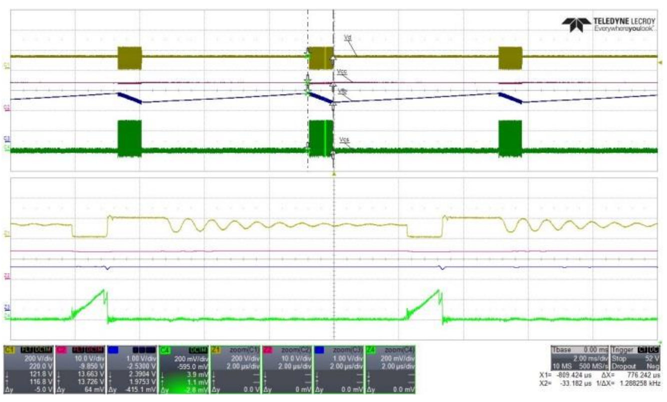
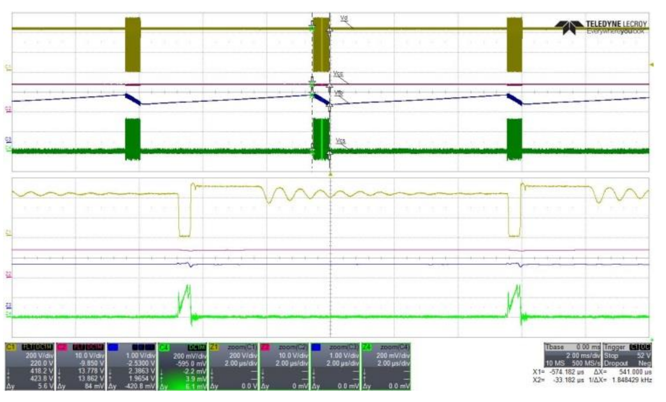
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
During ABM level 1: $V_{FB\_Bon\_ISO}$ = 2.4 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BHP} = 0.275 V (1 W load at 85 V AC)	During ABM level 1: $V_{FB\_Bon\_ISO}$ = 2.4 V, $V_{FB\_BOff\_ISO}$ = 2.0 V, V_{CS_BHP} = 0.275 V (1 W load at 300 V AC)

Figure 26 During ABM

11.10 Leaving ABM

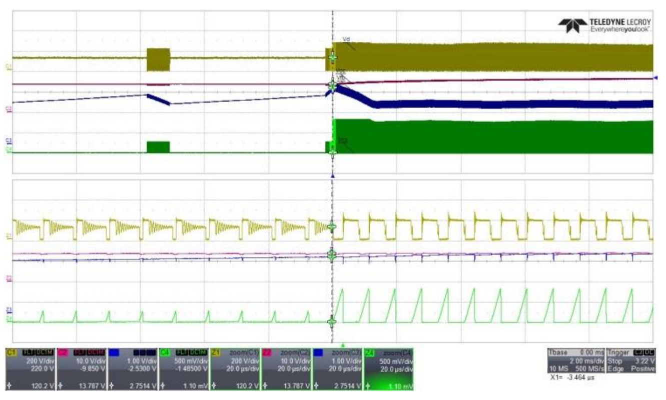
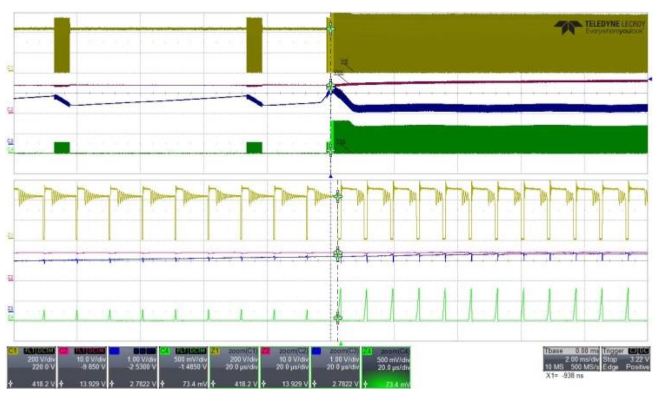
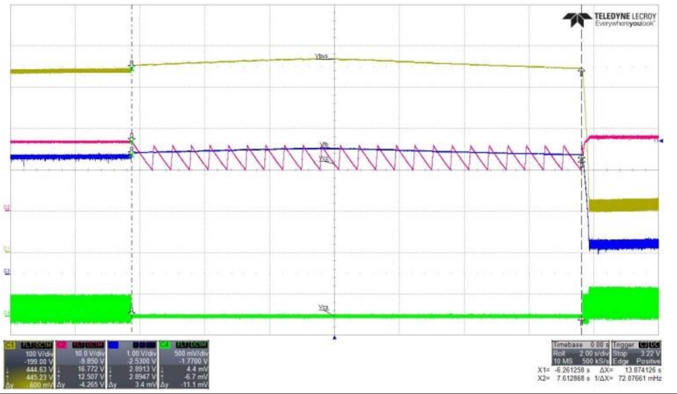
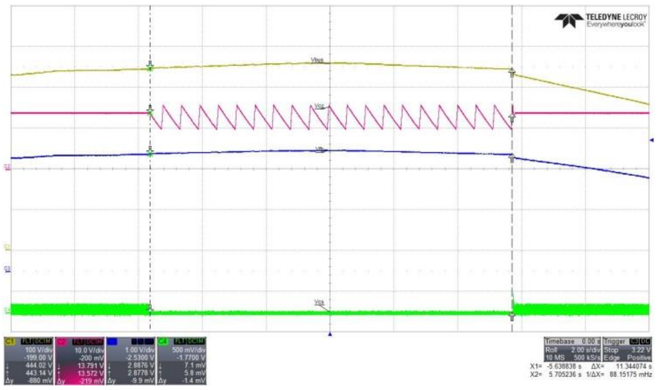
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to leave ABM level 3: V_{FB} > 2.75 V (load change from 1 W to full-load at 85 V AC)	Condition to leave ABM level 3: V_{FB} > 2.75 V (load change from 1 W to full-load at 300 V AC)

Figure 27 Leaving ABM

11.11 Line OVP (non-switch auto restart)





C1 (yellow) : Bus voltage (V_{Bus}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : VIN voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Bus voltage (V_{Bus}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : VIN voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})
Condition to detect line OVP: V_{VIN} > 2.9 V (V_{BULK} > 444 V DC [≈ 320 V AC]) Condition to reset line OVP: V_{VIN} < 2.9 V (V_{BULK} < 444 V)	
(Gradually increase AC-line voltage at full-load until line OVP detect and decrease AC-line until line OVP reset)	(Gradually increase AC-line voltage at 1 W load until line OVP detect and decrease AC-line until line OVP reset)

Figure 28 Line OVP

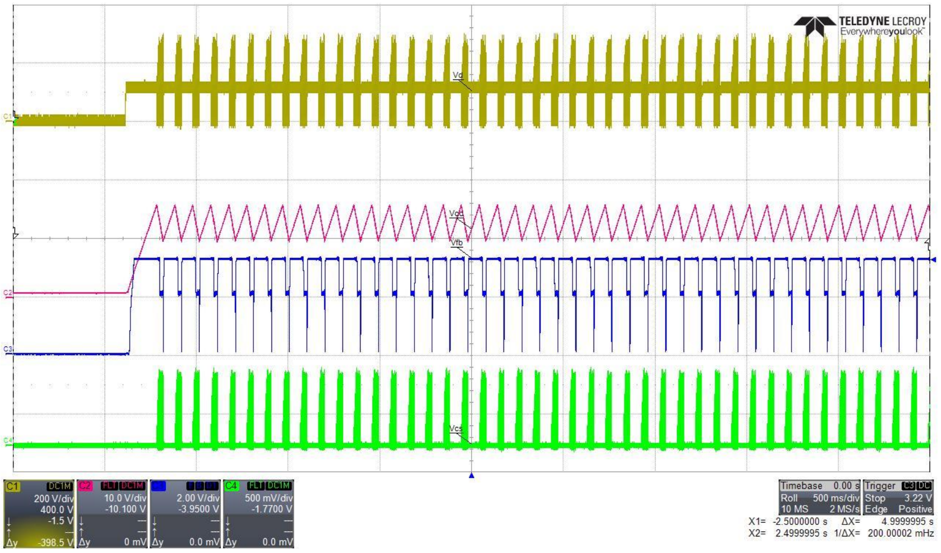
11.12 V_{CC} OVP (odd-skip auto restart)

C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} OVP: V_{VCC} > 25.5 V
(short R16A while system operating at 85 V AC and no-load)

Figure 29 V_{CC} OVP

11.13 V_{CC} under-voltage protection (auto restart)



C1 (yellow)	: Drain voltage (V_D)
C2 (purple)	: Supply voltage (V_{VCC})
C3 (blue)	: FB voltage (V_{FB})
C4 (green)	: CS voltage (V_{CS})

Condition to enter V CC under-voltage protection: V_{CC} < 10 V
(Remove R5 and power on the system with full-load at 85 V AC)

Figure 30 **V_{CC} under voltage protection**

11.14 Over-load protection (odd-skip auto restart)

C1 (yellow)	: Drain voltage (V_D)
C2 (purple)	: Supply voltage (V_{VCC})
C3 (blue)	: FB voltage (V_{FB})
C4 (green)	: CS voltage (V_{CS})

Condition to enter over-load protection: V_{FB} > 2.75 V and lasts for 54 ms blanking time
(load change from full- to short-load at 85 V AC)

Figure 31 **Over-load protection**

11.15 V_{CC} short-to-GND protection

C1 (yellow) : Drain voltage (V_D)
C2 (purple) : V CC voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : VIN voltage (V_{VIN})

Condition to enter V_{CC} short-to-GND: if $V_{CC} < V_{VCC\_SCP} \rightarrow I_{VCC} = I_{VCC\_Charge1}$
(Short V CC pin-to-GND and measure the current with multimeter before system start-up, $I_{VCC} \approx 300$ µA and input power is ≈ 40 mW at 85 V AC)

Figure 32 V_{CC} short-to-GND protection

12 References

[1] ICE5GSAG datasheet, Infineon Technologies AG

[2] 5^{th} Generation fixed frequency design guide

Revision history

Major changes since the last revision

Page or reference	Description of change
--	First release.

Edition 2018-02-25

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

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Document reference
AN_201702_PL83_005