# EZ-PD™ CCG7DC dual-port USB-C power delivery and DC-DC controller

## General description

EZ-PD™ CCG7DC is Infineon highly integrated dual-port USB Type-C power delivery (PD) solution with integrated buck-boost controllers. It complies to the latest USB Type-C and PD specifications, and is targeted for multi-port consumer charging applications. Integration offered by CCG7DC not only reduces the BOM but also provides a footprint optimized solution to support higher power density designs. CCG7DC has integrated gate drivers for VBUS NFET on the provider path. It also includes hardware-controlled protection features on the VBUS. CCG7DC supports a wide input voltage range (4 V to 24 V with 40 V tolerance) and programmable switching frequency (150 kHz to 600 kHz) in an integrated PD solution.

EZ-PD™ CCG7DC is the most programmable USB-PD solution with on-chip 32-bit Arm® Cortex®-M0 processor, 128-KB flash, 16-KB RAM and 32-KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as ADC, PWMs and Timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as dynamic load sharing and temperature monitoring.

## Applications

- Cigarette lighter adapter (CLA)
- Multi-port AC-DC charger and adapter
- Multi-port consumer charging applications

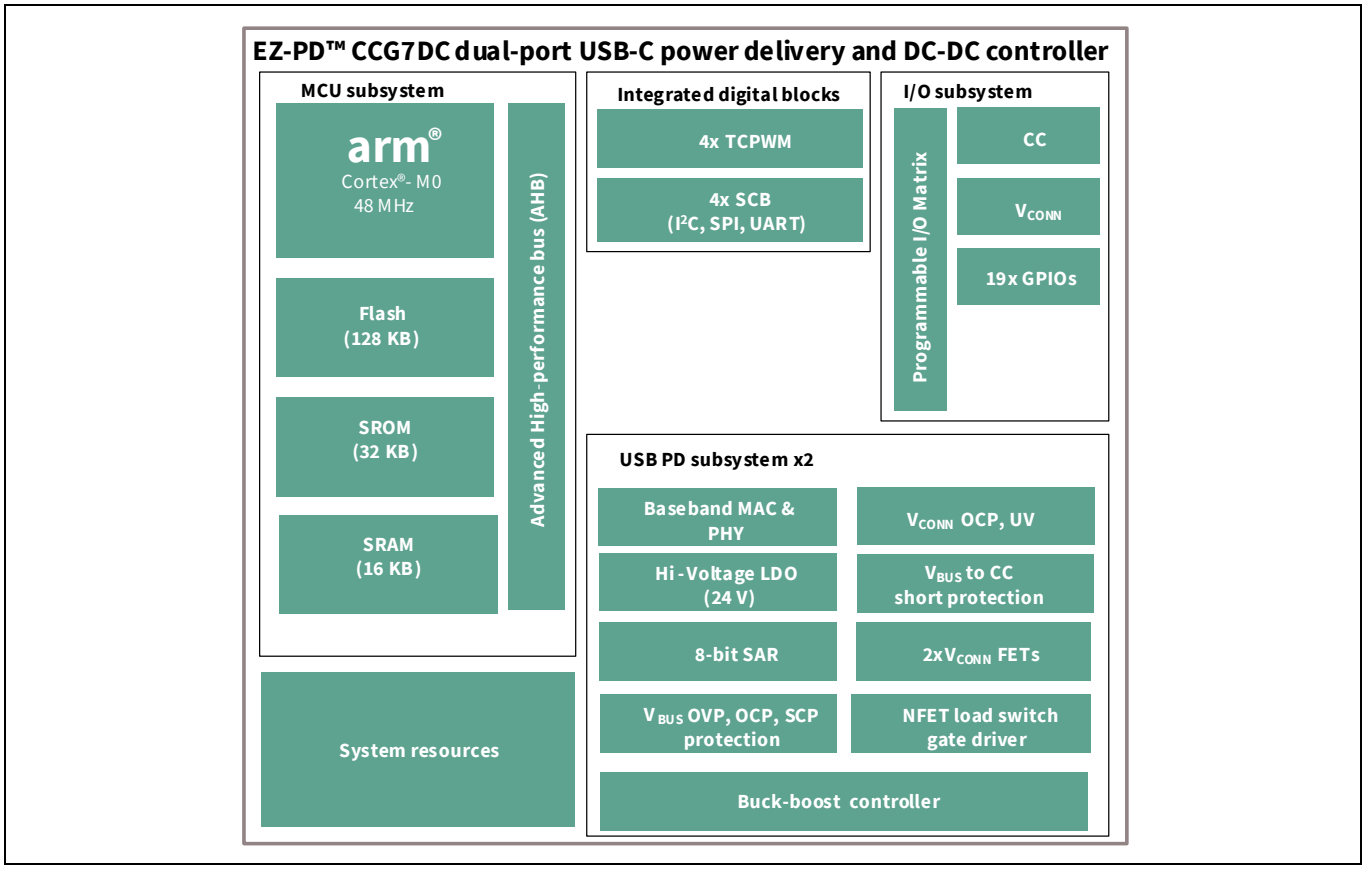
## Features

- USB-PD
  - Supports two USB-PD ports
  - Supports latest USB-PD 3.0 version 2.0 including programmable power supply (PPS) mode
  - Extended data messaging (EDM)
- Type-C
  - Configurable resistors RP and RD
  - VBUS NFET gate driver
  - Integrated 100-mW VCONN power supply and control
- 2x buck-boost controller
  - 150 kHz to 600 kHz switching frequency
  - 5.5 V to 24 V input, 40 V tolerant
  - 3.3 V to 21.5 V output
  - 20-mV voltage and 50-mA current steps for PPS
  - Supports selectable pulse skipping mode (PSM) and forced continuous conduction mode (FCCM)
  - Supports soft start
  - Programmable spread spectrum frequency modulation for low EMI
  - Programmable phase shift across two ports to further reduce the EMI
- 2x legacy/proprietary charging blocks
  - Supports QC4+, QC4.0, Samsung AFC, Apple 2.4A, and BC v1.2 charging protocols
- Integrated voltage (VBUS) regulation and current sense amplifier (CSA)
  - Integrated shunt regulator function for VBUS control
  - Constant current or constant voltage mode
  - Supports current sensing for constant current control

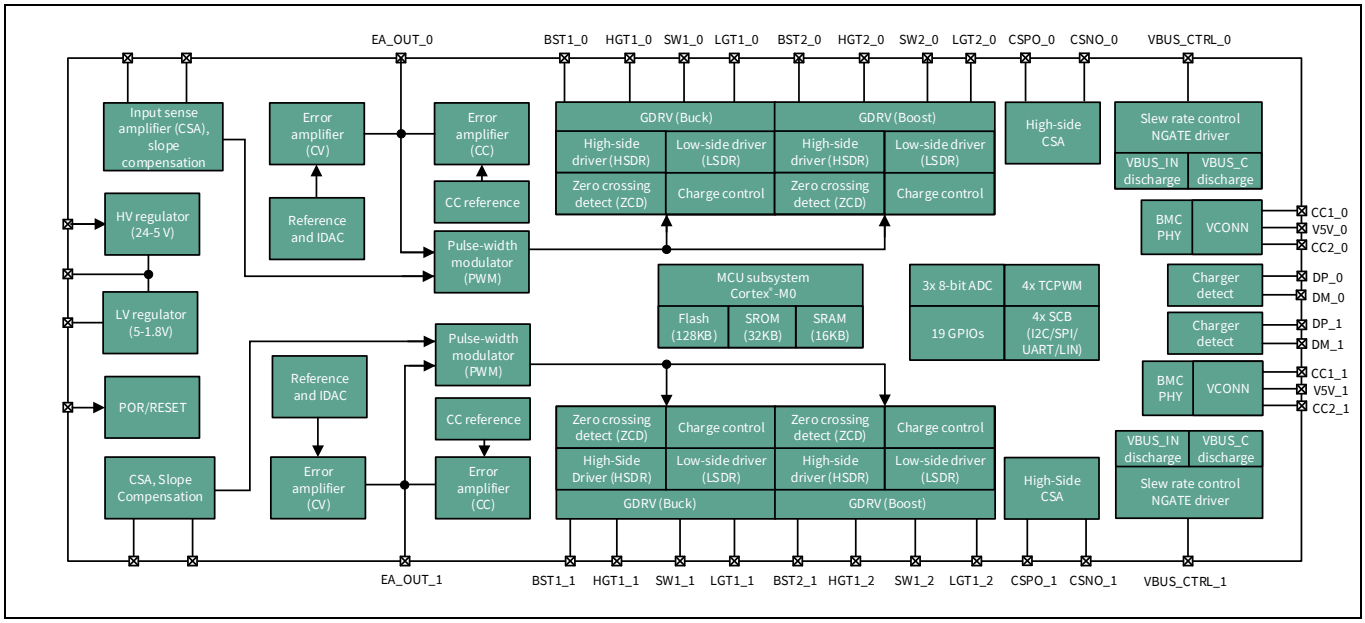
Features

- System-level fault protection
  - On-chip VBUS, overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
  - VBUS to CC short protection
  - Under-voltage lockout (UVLO)
  - Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
  - Supports connector and board temperature measurement using external thermistors
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0 CPU
  - 128-KB flash
  - 16-KB SRAM
  - 32-KB ROM
- Peripherals and GPIOs
  - 19 GPIOs
  - Two over-voltage GPIOs
  - 3x 8-bit ADC
  - 4x 16-bit timer/counter/PWMs (TCPWM)
- Communication interfaces
  - 4x SCBs ($I^2C$/SPI/UART)
- Clocks and oscillators
  - Integrated oscillator eliminating the need for an external clock
- Power supply
  - 4 V to 24 V input (40-V tolerant)
  - 3.3 V to 21.5 V output
  - Integrated LDO capable of 5 V @ 150 mA
- Packages
  - 68-pin QFN (8 mm × 8 mm) package with –40°C to +105°C extended industrial temperature range

## Logic block diagram




## Functional block diagram



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# 1 Functional overview

## 1.1 MCU subsystem

### 1.1.1 CPU

The Cortex®-M0 in EZ-PD™ CCG7DC devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from deepsleep mode.

### 1.1.2 Flash ROM and SRAM

EZ-PD™ CCG7DC devices have 128-KB flash and 32-KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as $I^2C$, SPI, and so on. That spares flash for user application. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest USB PD specifications and application needs.

The 16-KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

## 1.2 USB PD subsystem

This subsystem provides the interface to the Type-C USB port. This subsystem comprises:

- USB PD physical layer
- VCONN switches
- Under voltage (UVP), over voltage (OVP) on VBUS
- Output high-side CSA (HS CSA) for VBUS
- VBUS discharge control
- Gate driver for VBUS provider NFET
- Charger detection block for legacy charging
- VBUS to CC short-circuit protection

### 1.2.1 USB PD physical layer

The USB PD subsystem contains the USB PD physical layer block and supporting circuits. The USB PD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.0 standard. All communication is half-duplex. The physical layer or PHY practices collision avoidance to minimize communication errors on the channel.

Also, the USBPD block includes all termination resistors (Rp and Rd) and their switches as required by the USB Type-C spec. Rp and Rd resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The Rp resistor is implemented as a current source.

CCG7DC device family is fully complaint with revisions 3.0 and 2.0 of the USB PD specification. The device supports PPS operation at all valid voltages from 3.3 V to 21 V.

CCG7DC devices support Rp under HW control in unconnected (standby) state to minimize standby power.

CCG7DC devices support USB-PD extended messages containing data of up to 260 bytes. The extended messages are larger than expected by USB-PD 2.0 hardware. As per the USB-PD protocol specification, USB-PD 3.0 compliant devices implement a Chunking mechanism; messages are limited to Revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

### 1.2.2 VCONN switches

EZ-PD™ CCG7DC's internal LDO voltage regulator is capable of powering a 100mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories as defined in the USB Type-C specification. All circuitry including VCONN switches and over-current protection is integrated in the device. In the event the VCONN current exceeds the VCONN OCP limit, CCG7DC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.3 VBUS UVP and OVP

VBUS undervoltage and overvoltage faults are monitored using internal resistor dividers. The fault thresholds and response times are user configurable. Refer to the **EZ-PD™ Configuration Utility** for more details. In the event of a UVP or OVP, CCG7DC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.4 VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal CSAs. Similar to OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. Refer to the **EZ-PD™ Configuration Utility** for more details. In the event of OCP or SCP, CCG7DC can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

### 1.2.5 HS-CSA for VBUS

EZ-PD™ CCG7DC device family supports VBUS current measurement and control using an external resistor (5 mΩ) in series with the VBUS path. The voltage drop across this resistor is used to measure the average output current. The same resistor is also used to sense and precisely control the output current in the PPS current foldback mode of operation.

### 1.2.6 VBUS discharge control

The chip supports high-voltage (21.5 V) VBUS discharge circuitry. Upon the detection of device disconnection, faults, or hard resets, the chip will discharge the output VBUS terminals to vSafe5 V and/or vSafe0 V within the time limits specified in the USB PD specification.

### 1.2.7 Gate driver for VBUS provider NFET

EZ-PD™ CCG7DC devices have an integrated high-voltage gate driver to drive the gate of an external high-side NFET on the VBUS provider path. The gate driver drives the load switch that controls the connection between VBUS_IN and VBUS_C. VBUS_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives VBUS_IN low. To turn on the external NFET, it drives the gate to VBUS_IN + 8 V. There is an optional slow turn-on feature which is meant to avoid sudden in-rush current. For a typical gate capacitance of 3-nF, a slow turn-on time of 2 ms to 10 ms is configurable using firmware.

### 1.2.8 Legacy charge detection and support

The chip implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging, Qualcomm quick charge 2.0/3.0, Samsung AFC protocols and several upcoming proprietary charging protocols.

### 1.2.9 VBUS to CC short protection

EZ-PD™ CCG7DC's CC pins have integrated protection from accidental shorts to high-voltage VBUS. CCG7DC devices can handle up to 24 V external voltage on its CC pins without damage. In the event an over-voltage is detected on the CC pin, CCG7DC can be configured to shut down the Type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

## 1.3 Buck-boost subsystem

The buck-boost subsystem in EZ-PD™ CCG7DC devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. Buck-only mode is useful when CCG7DC device's port is used for multi-port AC/DC designs. **Figure 1** illustrates the buck-boost subsystem's main external components and connections.

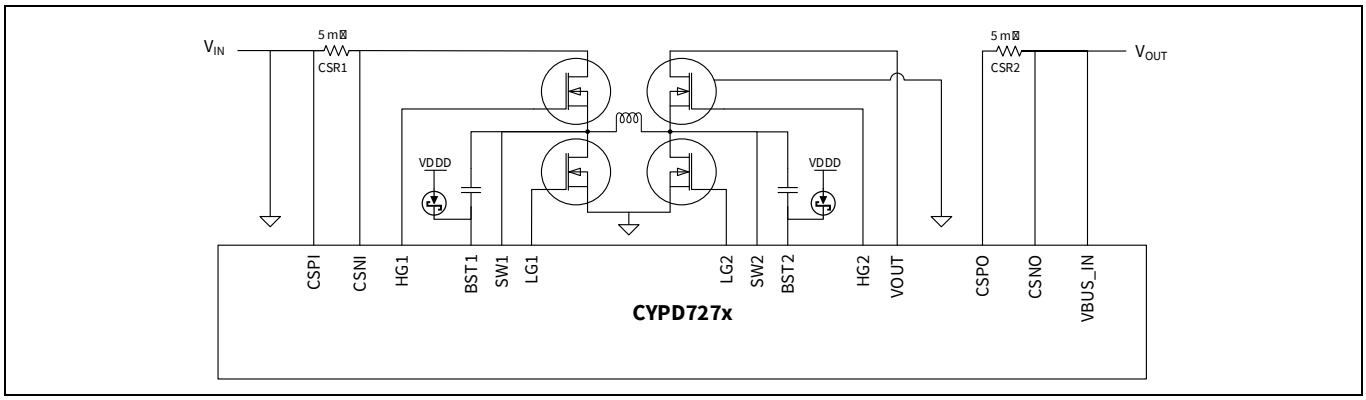



**Figure 1 Buck-boost schematic showing external components**

Buck-boost subsystem in EZ-PD™ CCG7DC devices have the following key functional blocks:

- High-side (cycle-by-cycle) CSA
- High-side and low-side gate driver
- Pulse-width modulator (PWM)
- Error amplifier (EA)

### 1.3.1 High-side (cycle-by-cycle) CSA

EZ-PD™ CCG7DC device's buck-boost controller implements peak current control in both boost and buck modes. A high-side CSA is used for peak current sensing through an external resistor (5 mΩ; see CSR1 in **Figure 1**) placed in series with the buck control FET. This CSA is high bandwidth and very wide common mode amplifier. This current sense resistor is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 1**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

### 1.3.2 High-side gate driver and low-side gate driver (HG/LG)

EZ-PD™ CCG7DC's buck-boost controller provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high-side gate drivers drive the high-side external FET with a nominal VGS of 5 V. The high-side gate driver has a programmable drive strength to drive external FET. An external capacitor and Schottky diode form a bootstrap network to collect and store the high voltage source (VIN + ~5 V for HG1 and VBUS + ~5 V for HG2) needed to drive the high-side FET.

The low-side gate driver drives the low-side external FET with a nominal VGS of 5 V using energy sourced from CCG7DC's internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive external FET.

In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5 V) provided the VIN voltage is between 5.5 V and 24 V.

### 1.3.3 Error amplifier (EA)

EZ-PD™ CCG7DC's buck-boost controller contains two error amplifiers for output voltage and current regulation. The error amplifier is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VBUS high-side CSA through the external resistor. The output of the VBUS CSA is compared with internal reference in error amplifier block and EA output is fed to the PWM block. CCG7DC devices negotiate a power delivery contract over the Type-C port in compliance to USB-PD specification with the peer sink device and in turn controls the EA output through the integrated programmable error amplifier circuit for achieving the required VBUS voltage output.

### 1.3.4 Pulse-width modulator (PWM)

EZ-PD™ CCG7DC device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

CCG7DC devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: PSM and FCCM. It is critical in charger applications where the load can vary from a few watts to 100 W.

### 1.3.5 Pulse skipping mode (PSM)

In pulse skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ CCG7DC devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the CCG7DC devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

### 1.3.6 Forced continuous conduction mode (FCCM)

In forced continuous conduction mode, the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

## 1.4 Buck-boost controller operation regions

The CSA output is compared with the output of the error amplifier to determine the pulse width of the PWM. PWM block compares the Input voltage and output voltage to determine the buck, boost, and buck-boost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VIN vs VOUT thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

### 1.4.1 Buck region operation (VIN >> VBUS)

When the VIN voltage is significantly higher than the required VBUS voltage, EZ-PD™ CCG7DC devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 2**. Depending on the application and requirement the device can be configured to operate in buck mode only at all times using only two FETs.

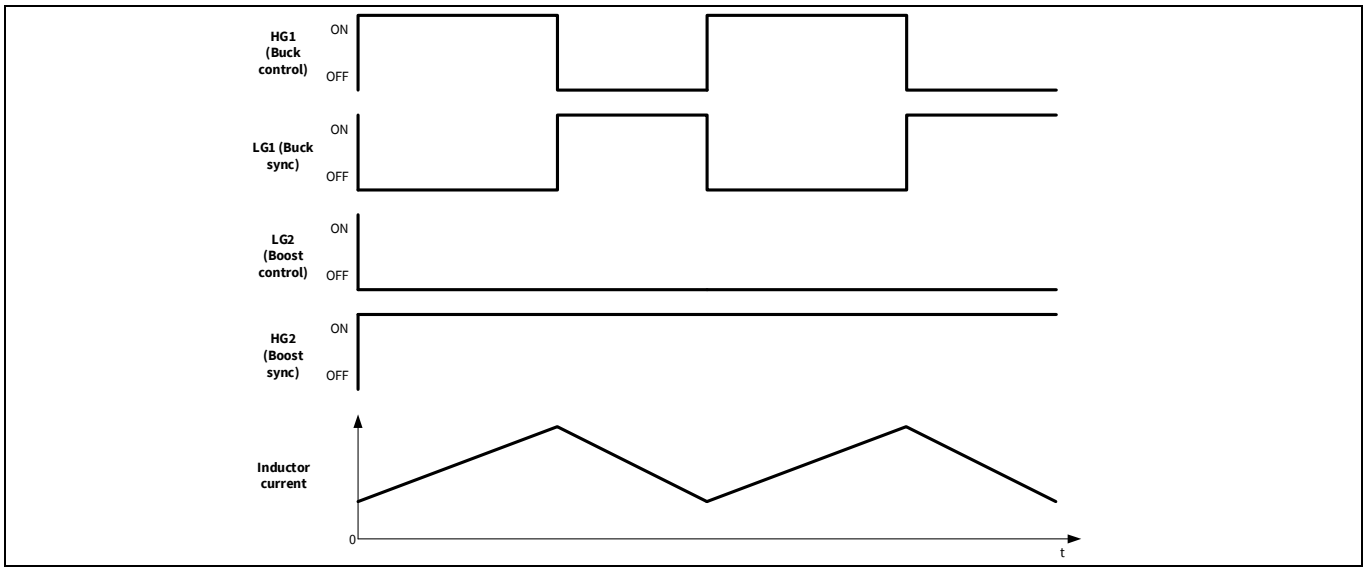



**Figure 2 Buck operation waveforms**

### 1.4.2 Boost region operation (VIN << VBUS)

When the VIN voltage is significantly lower than the required VBUS voltage, EZ-PD™ CCG7DC devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned OFF and the buck control FET turned ON. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 3**.

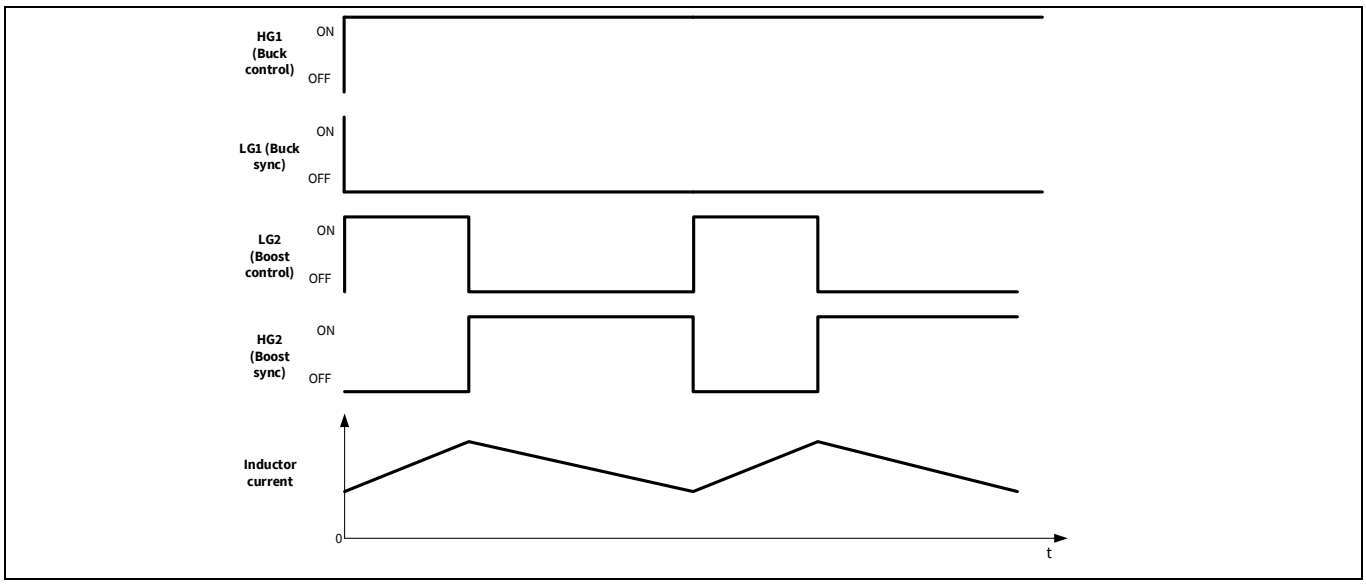



**Figure 3 Boost operation waveforms**

### 1.4.3 Buck-boost region 1 operation (VIN ~> VBUS)

When the VIN voltage is slightly higher than the required VBUS voltage, EZ-PD™ CCG7DC devices operate in the buck-boost region 1. In this region, the boost side FET (LG2) works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 4**.

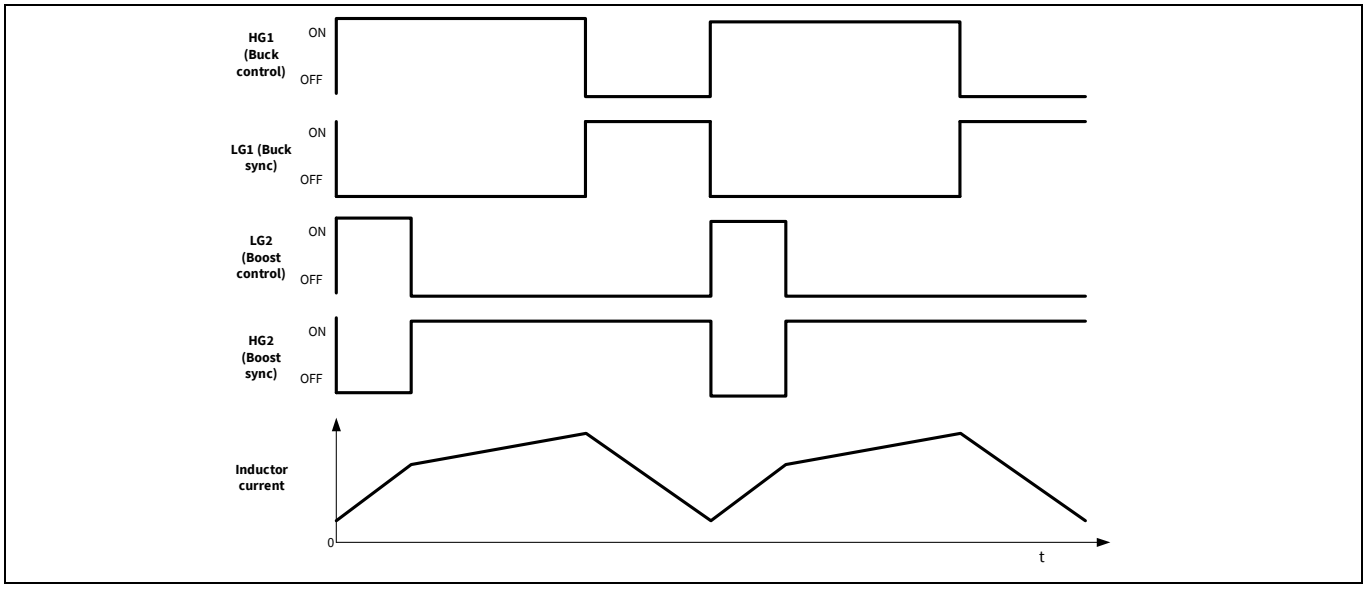



**Figure 4 Buck-boost region 1 (VIN ~> VBUS) operation waveforms**

### 1.4.4 Buck-boost region 2 operation (VIN ~< VBUS)

When the VIN voltage is slightly lower than the required VBUS voltage, EZ-PD™ CCG7DC devices operate in the buck-boost region 2. In this region, the buck side (HG1) works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 5**.

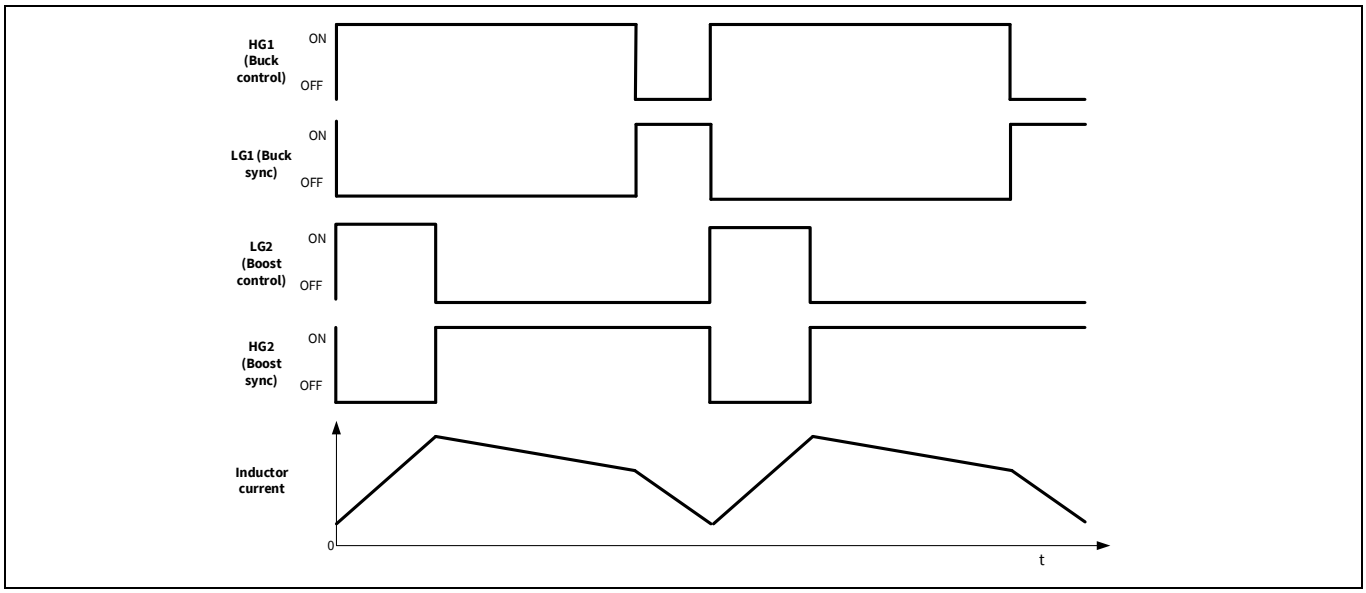



**Figure 5 Buck-boost region 2 (VIN ~< VBUS) operation waveforms**

### 1.4.5 Switching frequency and spread spectrum

EZ-PD™ CCG7DC devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

## 1.5 Analog blocks

### 1.5.1 ADC

CCG7DC devices family have three 8-bit SAR ADCs available for general purpose A-D conversion applications in the chip. The ADCs can be accessed from the GPIOs through an on-chip analog mux. See **Table 26** for detailed specs on the ADCs.

## 1.6 Integrated digital blocks

### 1.6.1 Serial communication block (SCB)

EZ-PD™ CCG7DC devices have four SCB blocks that can be configured for $I^2C$, SPI, or UART. These blocks implement full multi-master and slave $I^2C$ interfaces capable of multi-master arbitration. $I^2C$ is compatible with the standard Philips $I^2C$ specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The $I^2C$ port I/Os for SCB0 are over-voltage tolerant (OVT). The $I^2C$ ports for SCB1-3 are not OVT compliant.

### 1.6.2 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ CCG7DC devices support four timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

## 1.7 I/O subsystem

The EZ-PD™ CCG7DC devices have 19 GPIOs including the I2C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight drive strength modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control.
- OVT on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed in order to reduce internal multiplexing complexity. Data Output registers and Pin State register store, respectively, the values to be driven on the pins and the states of the pins themselves. The configuration of the pins can be done by the programming of registers through software for each digital I/O port.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during deepsleep mode or remain ON. If the operation is restored using reset, then the pins shall go the high-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

## 1.8 System resources

### 1.8.1 Watchdog timer (WDT)

EZ-PD™ CCG7DC devices have a watchdog timer running from the internal low-speed oscillator (ILO). This allows watchdog operation during deepsleep and generate a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

### 1.8.2 Reset

EZ-PD™ CCG7DC devices can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The Reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. XRES pin is the dedicated pin for reset to apply hardware reset.

### 1.8.3 Clock system

CCG7DC devices have a fully integrated clock with no external crystal required. CCG7DC device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources, without glitches.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N is the divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In **Figure 6**, PERXYZCLK represents the clocks for different peripherals.

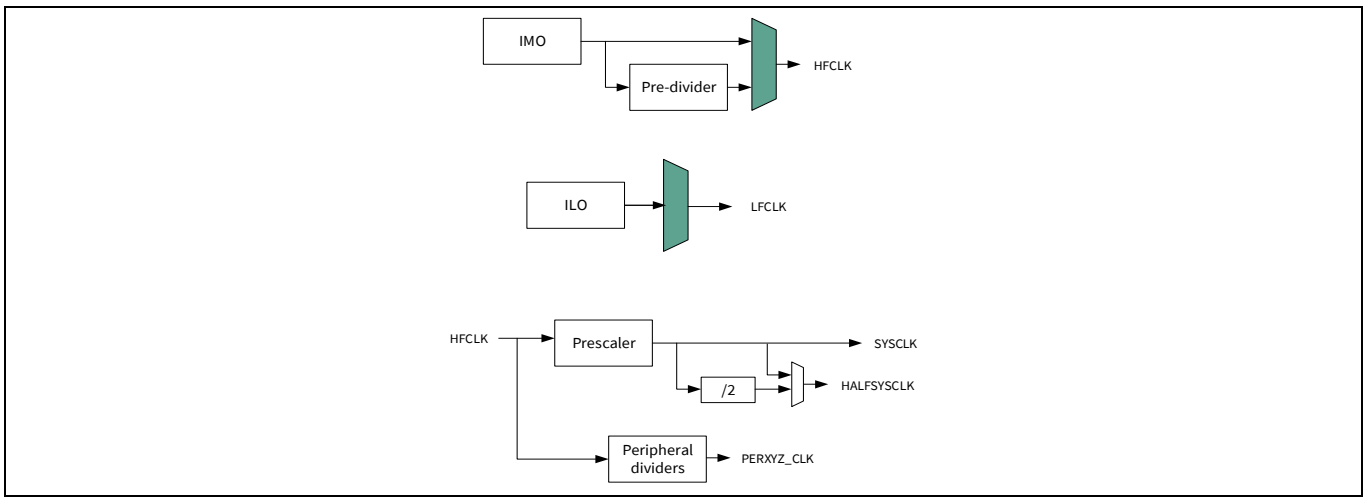



**Figure 6 Clocking architecture of EZ-PD™ CCG7DC devices**

### 1.8.4 Internal main oscillator (IMO) clock source

The internal main oscillator is the primary source of internal clocking in CCG7DC devices. IMO default frequency for CCG7DC devices is 48 MHz ± 2%.

### 1.8.5 ILO clock source

The internal low-speed oscillator is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB suspend (deepsleep) mode.

# 2 Power subsystem

**Figure 7** illustrates an overview of the power subsystem architecture for EZ-PD™ CCG7DC devices. The power subsystem of CCG7DC devices operate from VIN supply which can vary from 4 V to 24 V. The VDDD pin, the output of 5 V LDO gets input from VIN supply. The VDDD pin can also be used as a power supply for external loads up to 150 mA. CCG7DC devices have two different power modes: Active and deepsleep, transitions between which are managed by the power system. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-µF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.

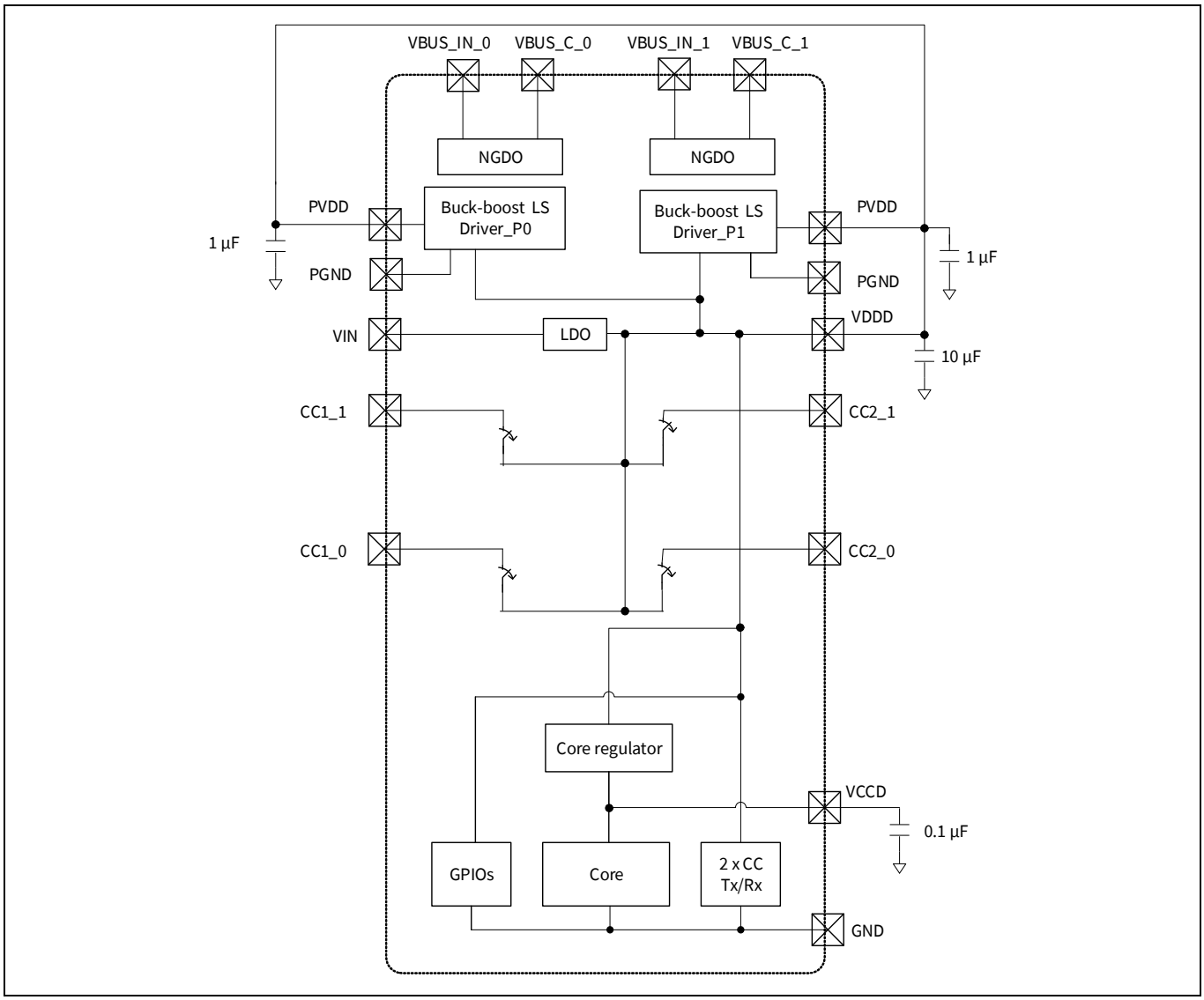



**Figure 7 Power system requirement block diagram**

## 2.1 VIN undervoltage lockout (UVLO)

EZ-PD™ CCG7DC supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

## 2.2 Using external VDDD supply

By default, external VDDD is not supported for CCG7DC devices. However, usage of external VDDD supply can be enabled using firmware. The pre-requisite for enabling external forcing of VDDD is to always maintain VIN higher than VDDD and the external load on VDDD pin of CCG7DC devices should never be higher than prescribed load capability of internal VDDD LDO.

## 2.3 Power modes

The power modes of the device accessible and observable by the user are shown in **Table 1**.

**Table 1 Power modes**

| Mode | Description |
|---|---|
| RESET | Power is valid and XRES is not asserted. An internal reset source is asserted or sleep controller is sequencing the system out of reset. |
| ACTIVE | Power is valid and CPU is executing instructions. |
| SLEEP | Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power. |
| DEEPSLEEP | Main regulator and most hard-IP are shut off. Deepsleep regulator powers logic, but only low-frequency clock is available. |
| XRES | Power is valid and XRES is asserted. Core is powered down. |

# 3 Pin information

**Table 2 EZ-PD™ CCG7DC pinout table**

| Pin# | Pin name | GPIO port | Description |
|---|---|---|---|
| 1 | SW1_0 | – | Negative power rail of port 0 buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection. |
| 2 | LG1_0 | | Buck low-side gate driver output of port 0. Connect to the buck (input) side sync (low-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 3 | PGND_0 | | Ground of low-side gate driver of port 0. This is also connected to one input terminal of ZCD of buck low-side gate driver. Connect directly to port 0's board ground plane. |
| 4 | PVDD_0 | | Supply of low-side gate driver of port 0. Connect to VDDD. Use 1-µF and 0.1-µF bypass capacitors as close to the CCG7DC IC as possible. |
| 5 | LG2_0 | | Boost low-side gate driver output of port 0. Connect to the boost (output) side control (low-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 6 | VOUT_0 | | Output of the buck-boost converter of port 0. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the boost sync (high-side) FET's drain. Use a dedicated (Kelvin) trace for this connection. |
| 7 | SW2_0 | | Negative power rail of port 0 boost high-side gate driver. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection. |
| 8 | HG2_0 | | Boost high-side gate driver output of port 0. Connect to the boost (output) side sync (high-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 9 | BST2_0 | | Boosted power supply of port 0 boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2_0. Also, connect a bootstrap capacitor from this pin to SW2_0. |
| 10 | COMP_0 | | EA output pin of port 0. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network. |
| 11 | CSPO_0 | | Positive input of output CSA of port 0. Connect to positive terminal of the output current sense resistor. |
| 12 | CSNO_0 | | Negative input of output CSA of port 0 Connect to negative terminal of the output current sense resistor. |
| 13 | VBUS_IN_0 | | Input of feedback voltage of EA of port 0. Connect to the VBUS node between the output current sense resistor and the VBUS Provider NFET. |
| 14 | VBUS_C_0 | | Type-C connector VBUS voltage of port 0. Connect to the Type-C connector's VBUS pin. |
| 15 | CC1_0 | | Type-C connector configuration channel 1 of port 0. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground. |

**Table 2 EZ-PD™ CCG7DC pinout table** *(continued)*

| Pin# | Pin name | GPIO port | Description |
|---|---|---|---|
| 16 | CC2_0 | – | Type-C connector configuration channel 2 of port 0. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground. |
| 17 | VBUS_CTRL_0 | | VBUS NFET gate driver output of port 0. Connect to the provider NFET's gate. |
| 18 | CSN_0_GPIO0 | P0.0 | GPIO |
| 19 | CSP_0_GPIO1 | P0.1 | |
| 20 | GPIO2 | P0.2 | |
| 21 | GPIO3 | P0.3 | |
| 22 | GPIO4 | P0.4 | |
| 23 | DP_0_GPIO5 | P1.0 | USB D+ of port 0/GPIO: D+ for implementing BC 1.2, AFC, QC or Apple Charging.<br>CCG7DC does not support USB data transmission on this pin. |
| 24 | DM_0_GPIO6 | P1.1 | USB D- of port 0/GPIO: D- for implementing BC 1.2, AFC, QC or Apple Charging.<br>CCG7DC does not support USB data transmission on this pin. |
| 25 | VDDD | – | 5-V LDO output. Connect a 1-µF ceramic bypass capacitor to this pin. Also, connect this pin directly to pin 63. |
| 26 | DM_1_GPIO7 | P1.2 | USB D- of port 1/GPIO: D- for implementing BC 1.2, AFC, QC or Apple Charging. CCG7DC does not support USB data transmission on this pin. |
| 27 | DP_1_GPIO8 | P1.3 | USB D+ of port 1/ GPIO: D+ for implementing BC 1.2, AFC, QC or Apple Charging. CCG7DC does not support USB data transmission on this pin. |
| 28 | XRES | – | External reset – active low. Contains a 3.5 kΩ to 8.5 kΩ internal pull-up. |
| 29 | GPIO9 | P2.0 | GPIO |
| 30 | GPIO10 | P2.1 | |
| 31 | GPIO11 | P1.4 | |
| 32 | CSP_1_GPIO12 | P1.5 | |
| 33 | CSN_1_GPIO13 | P1.6 | |
| 34 | GND | – | Chip ground. Connect directly to the exposed pad (EPAD) and to pin 64. |
| 35 | VBUS_CTRL_1 | | VBUS NFET gate driver output of port 1. Connect to the provider NFET's gate. |
| 36 | CC2_1 | | Type-C connector configuration channel 2 of port 1. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground. |
| 37 | CC1_1 | | Type-C connector configuration channel 1 of port 1. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground. |
| 38 | VBUS_C_1 | | Type-C connector BUS voltage of port 1. Connect to the Type-C connector's VBUS pin. |
| 39 | VBUS_IN_1 | | Input of feedback voltage of EA of port 1. Connect to the VBUS node between the output current sense resistor and the VBUS provider NFET. |

**Table 2 EZ-PD™ CCG7DC pinout table** *(continued)*

| Pin# | Pin name | GPIO port | Description |
|---|---|---|---|
| 40 | CSNO_1 | – | Negative input of output CSA of port 1. Connect to negative terminal of the output current sense resistor. |
| 41 | CSPO_1 | | Positive input of output CSA of port 1. Connect to positive terminal of the output current sense resistor. |
| 42 | COMP_1 | | EA output pin of port 1. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network. |
| 43 | BST2_1 | | Boosted power supply of port 1 boost high-side gate driver. Connect Schottky diode from VDDD to BST2_1. Bootstrap capacitor node. Also, connect a bootstrap capacitor from this pin to SW2_1. |
| 44 | HG2_1 | | Boost high-side gate driver output of port 1. Connect to the boost (output) side sync (high-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 45 | SW2_1 | | Negative power rail of port 1 boost high-side gate driver. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection. |
| 46 | VOUT_1 | | Output of the buck-boost converter of port 1. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the boost sync (high-side) FET's drain. Use a dedicated (Kelvin) trace for this connection. |
| 47 | LG2_1 | | Boost low-side gate driver output of port 1. Connect to the boost (output) side control (low-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 48 | PVDD_1 | | Supply of low-side gate driver of port 1. Connect to VDDD. Use a 1 µF and 0.1 µF bypass capacitors as close to the CCG7DC device as possible. |
| 49 | PGND_1 | | Ground of low-side gate driver of port 1. This is also connected to one input terminal of zero current detection of buck low-side gate driver.<br>Connect directly to Port 0's board ground plane. |
| 50 | LG1_1 | | Buck low-side gate driver output of port 1. Connect to the buck (input) side sync (low-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 51 | SW1_1 | | Negative power rail of port 1 buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection. |
| 52 | HG1_1 | | Buck high-side gate driver output of port 1. Connect to the buck (input) side control (high-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| 53 | BST1_1 | | Boosted power supply of port 1 buck high-side gate driver. Connect Schottky diode from VDDD to BST1_1. Bootstrap capacitor node. |
| 54 | CSNI_1 | | Negative input of input CSA of port 1. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection. |
| 55 | CSPI_1 | | Positive input of input CSA of port 1. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection. |

**Table 2 EZ-PD™ CCG7DC pinout table** *(continued)*

| Pin# | Pin name | GPIO port | Description |
|---|---|---|---|
| 56 | GPIO14/SWD_DAT | P3.0 | GPIO/SWD programming and debug data signal |
| 57 | GPIO15/SWD_CLK | P3.1 | GPIO/SWD programming and debug clock signal |
| 58 | GPIO16 | P3.2 | GPIO |
| 59 | GPIO17 | P3.3 | |
| 60 | GPIO18 | P3.4 | |
| 61 | VIN | – | 4 V–24 V input supply. Connect a ceramic bypass capacitor to GND close to this pin. |
| 62 | VCCD | | 1.8-V core LDO output. Connect a 0.1-µF bypass capacitor to ground. Do not connect anything else to this pin. |
| 63 | VDDD | | 5-V LDO output. Connect to pin 25. Also connect a 10-µF bypass capacitor to this pin. |
| 64 | GND | | Chip ground. Connect to the EPAD and to pin 34. |
| 65 | CSPI_0 | | Positive input of input CSA of port 0. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection. |
| 66 | CSNI_0 | – | Negative input of input CSA of port 0. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection. |
| 67 | BST1_0 | | Boosted power supply of port 0 buck high-side gate driver. Bootstrap capacitor node.<br>Connect Schottky diode from VDDD to BST1_0. Also, connect a bootstrap capacitor from this pin to SW1_0. |
| 68 | HG1_0 | | Buck high-side gate driver output of port 0. Connect to the buck (input) side control (high-side) FET gate. Use a wide trace to minimize inductance of this connection. |
| | EPAD | | Exposed ground pad. Connect directly to pins 34 and 64. |

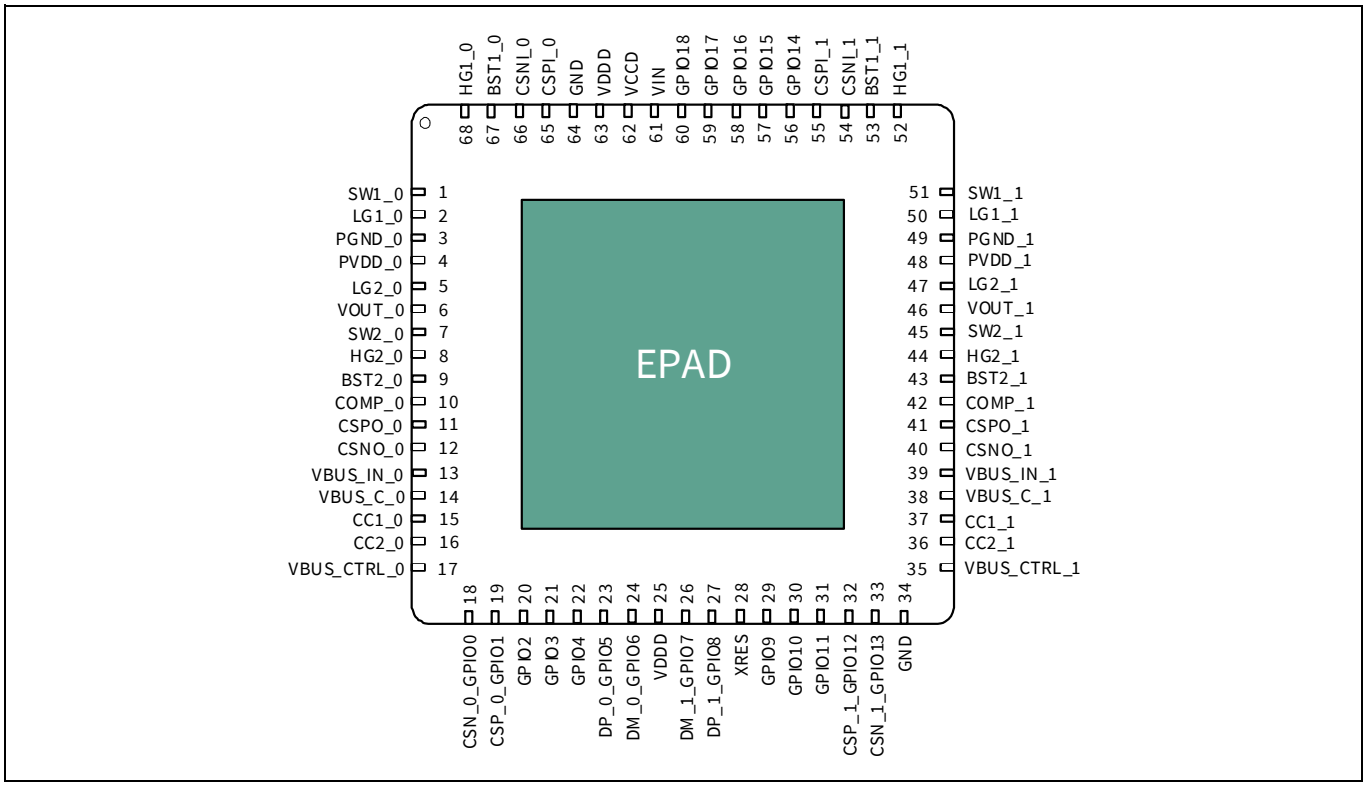



**Figure 8 CCG7DC 68-pin QFN pinout**

# 4 EZ-PD™ CCG7DC programming and bootloading

There are two ways to program application firmware into a CCG7DC device:

1. Programming the device flash over SWD interface
2. Application firmware update over specific interfaces (CC, I2C)

Generally, the CCG7DC devices are programmed over SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the CCG7DC device's application firmware can be updated via the appropriate bootloader interface. Infineon strongly recommends customers to use the **EZ-PD™ Configuration Utility** to turn off the application FW Update over CC or I2C interface in the firmware that is updated into CCG7DC's flash before mass production. This prevents unauthorized firmware from being updated over CC interface in the field. If you desire to retain the application firmware update over CC/I2C interfaces feature post-production for on-field firmware updates, contact **Infineon Sales** for further guidelines.

## 4.1 Programming the device flash over SWD interface

The CCG7DC family of devices can be programmed using the SWD interface. Infineon provides programming kits (**CY8CKIT-002 MiniProg3 Kit**) called MiniProg3 and (**CY8CKIT-005 MiniProg4 Kit**) MiniProg4 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This *hex* file is a binary file generated as an output of building the firmware project in **PSoC Creator Software**. Click **here** for more information on how to use the MiniProg3 programmer. Click **here** for more information on how to use the MiniProg4 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in **Figure 9**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pins of CCG7DC device. If the CCG7DC device is powered using an on-board power supply, it can be programmed using the "reset programming" option. More details will be provided in the CCG7XXX programming specifications once it is available.

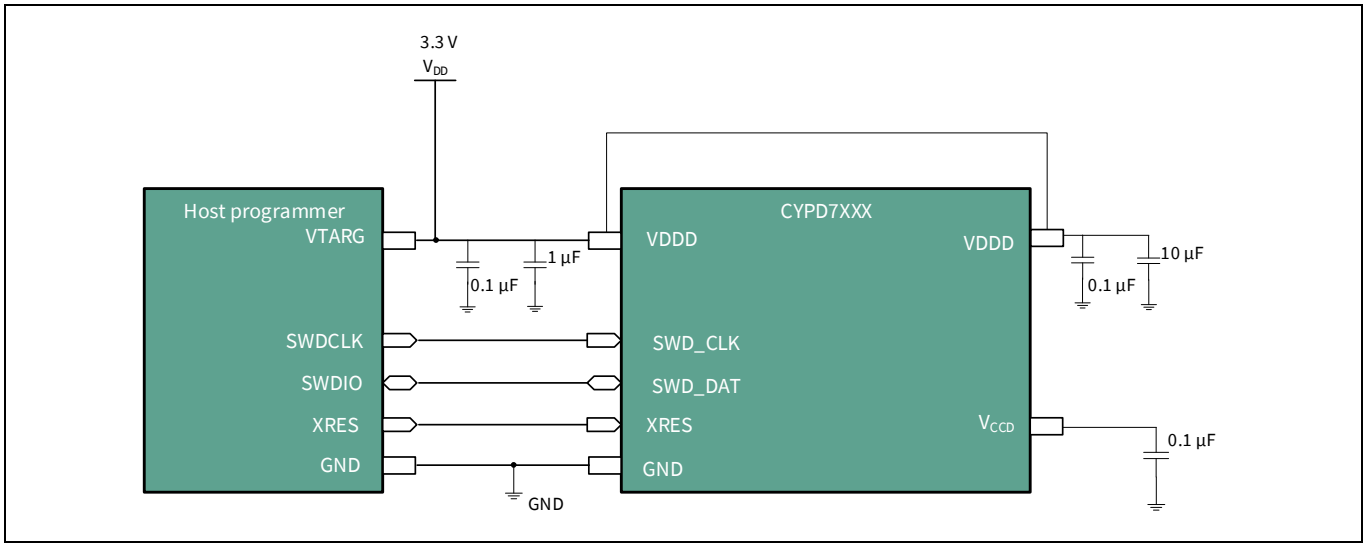



**Figure 9 Connecting the programmer to CYPD7XXX device**

# 5 Applications

**Figure 10** illustrates a multi-port cigarette lighter adapter (CLA) application block diagram using EZ-PD™ CCG7DC. CLA is powered by the car battery and is used for charging the mobile/tablet/notebook. In this application, CCG7DC will always be in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck-boost controller to supply the required voltage and current.

The DP/DM lines of the Type-C receptacles are connected to CCG7DC to support legacy charging protocols such as QC3.0, Samsung AFC, Apple 2.4A charging, BC v1.2, and so on. When no load is connected to the USB Type-C port, CCG7DC remains in Standby mode without switching on the buck-boost controller.

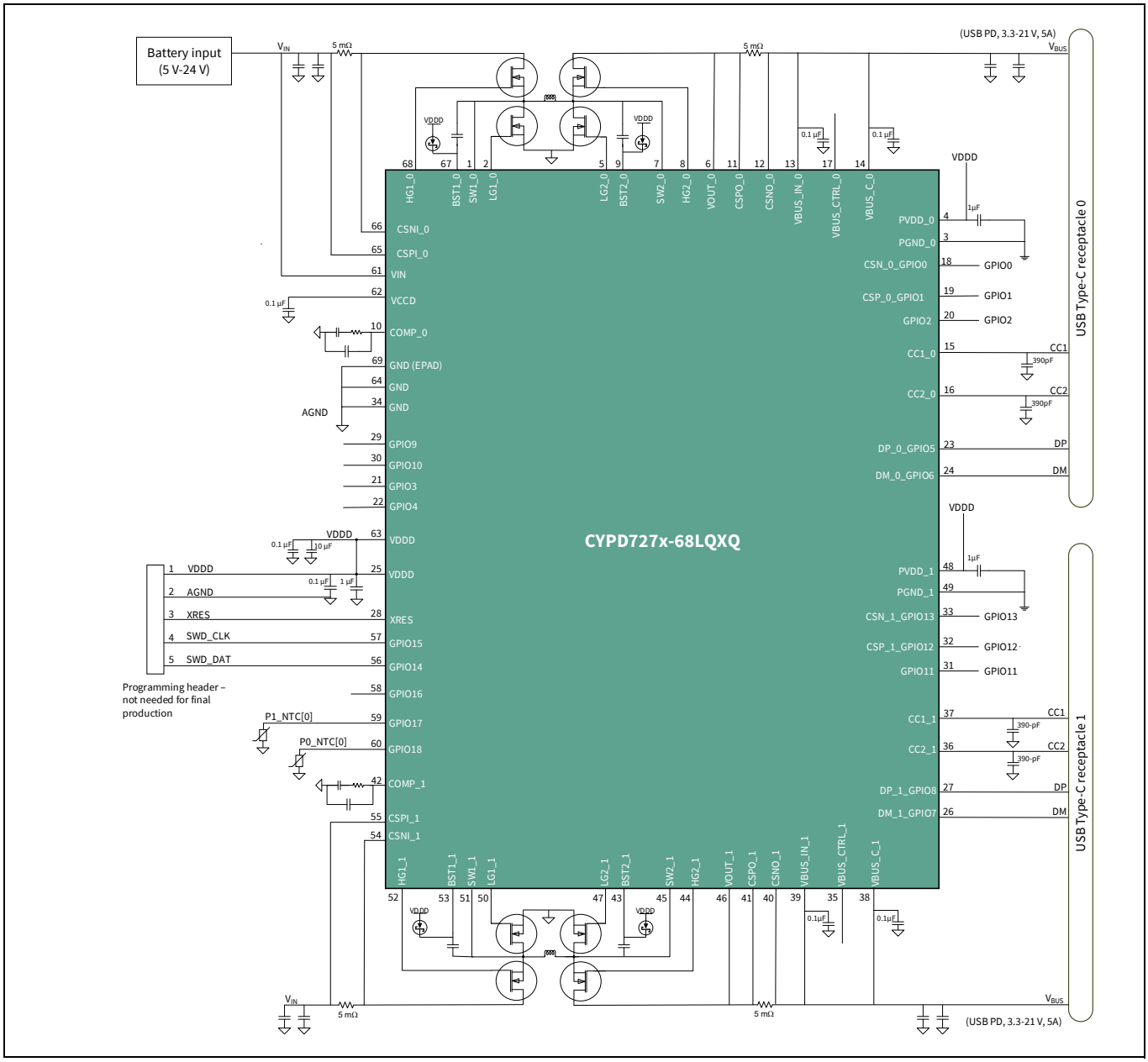



**Figure 10 EZ-PD™ CCG7DC CLA application diagram**

**Table 3 CLA GPIO pin mapping for application diagram in Figure 10**

| Pin # | Pin name | Function | GPIO | CLA |
|---|---|---|---|---|
| 18 | GPIO0 | General purpose IO, available for system level function | P0.0 | GPIO |
| 19 | GPIO1 | | P0.1 | |
| 20 | GPIO2 | | P0.2 | |
| 21 | GPIO3 | | P0.3 | |
| 22 | GPIO4 | | P0.4 | |
| 23 | DP_0_GPIO5 | Port 0: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC. | P1.0 | P0_DP |
| 24 | DM_0_GPIO6 | | P1.1 | P0_DM |
| 26 | DM_1_GPIO7 | Port 1: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC. | P1.2 | P1_DM |
| 27 | DP_1_GPIO8 | | P1.3 | P1_DP |
| 29 | GPIO9 | General purpose IO, available for system level function | P2.0 | GPIO |
| 30 | GPIO10 | | P2.1 | |
| 31 | GPIO11 | | P1.4 | |
| 32 | GPIO12 | | P1.5 | |
| 33 | GPIO13 | | P1.6 | |
| 56 | GPIO14 | Connect to the host programmer's SWDIO (data) for programming the CCG7DC device | P3.0 | |
| 57 | GPIO15 | Connect to the host programmer's SWDCLK (clock) for programming the CCG7DC chip enable pin | P3.1 | CHIP_EN |
| 58 | GPIO16 | GPIO, available for system level function | P3.2 | GPIO |
| 59 | GPIO17 | Port 1: Thermistor | P3.3 | P1_NTC[0] |
| 60 | GPIO18 | Port 0: Thermistor | P3.4 | P0_NTC[0] |

**Figure 11** illustrates a two Type-C port AC/DC power adapter application block diagram using CCG7DC. In this application, CCG7DC will always be in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck controller to supply the required voltage and current. The efficiency can be optimized by dynamically controlling the opto-coupler feedback and thereby regulate the buck input voltage to the closest output voltage. This application can be configured to support the legacy charging protocols - BC1.2 DCP, Qualcomm QC2.0/3.0, Apple Charging, and Samsung AFC.

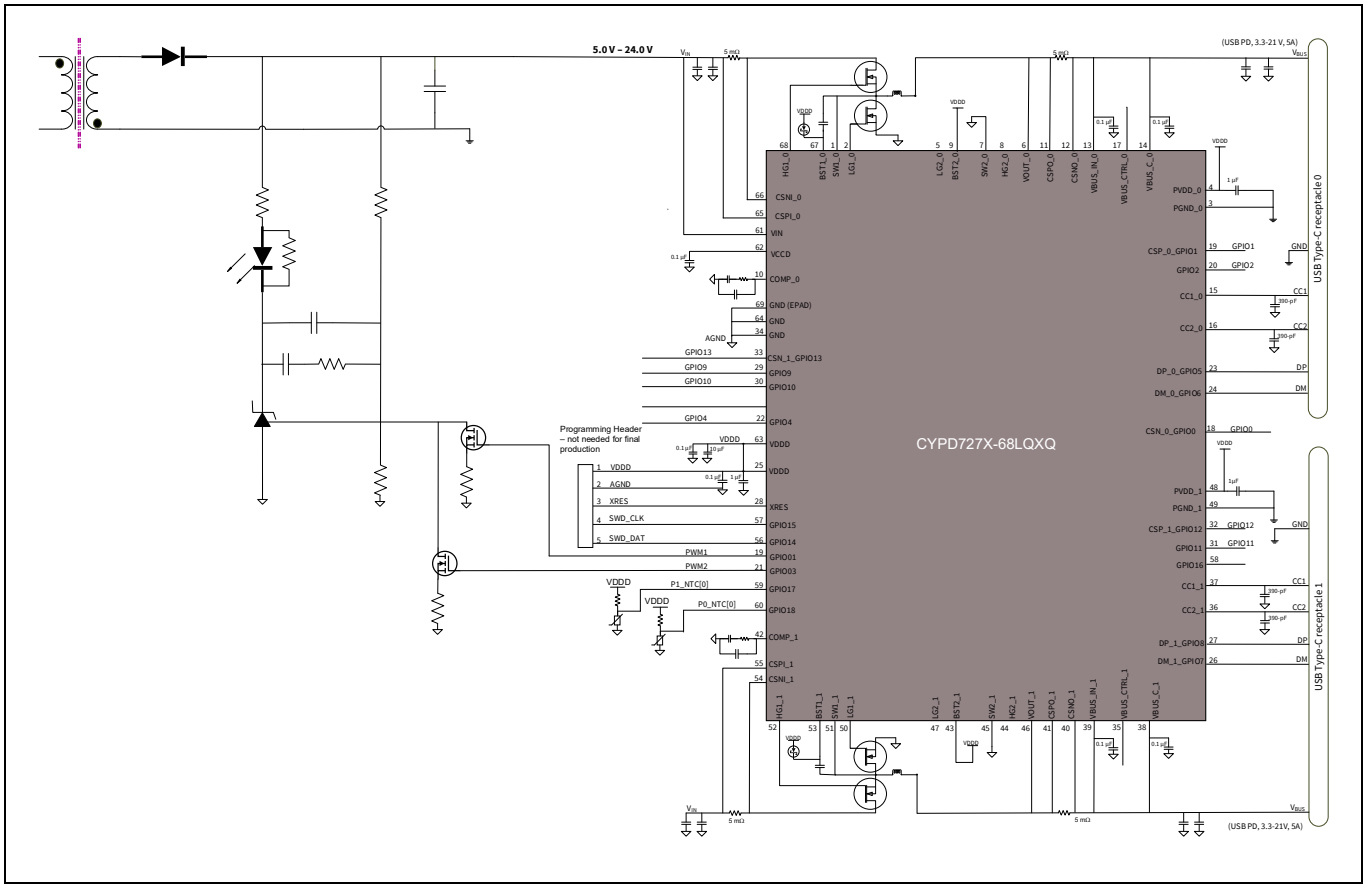



**Figure 11 EZ-PD™ CCG7DC multi-port AC-DC adapter application diagram**

# 6 Electrical specifications

## 6.1 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 4 Absolute maximum ratings**[1]

| Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|
| VIN_MAJ | Maximum input supply voltage | – | – | 40 | V | – |
| VDDD_MAJ | Maximum supply voltage relative to VSS | | | 6 | | |
| V5V_MAJ | Maximum supply voltage relative to VSS | | | | | |
| VBUS_C_MAJ | Max $_{VBUS\_C}$ (P0/P1) voltage relative to Vss | | | 24 | | |
| VCC_PIN_ABS | Max voltage on CC1 and CC2 pins | | | | | |
| VGPIO_ABS | Inputs to GPIO | –0.5 | | VDDD + 0.5 | | |
| VGPIO_OVT_ABS | OVT GPIO Voltage | –0.5 | | 6 | | |
| IGPIO_ABS | Maximum current per GPIO | –25 | | 25 | mA | |
| IGPIO_INJECTION | GPIO injection current, max for VIH > VDDD, and Min for VIL < VSS | –0.5 | | 0.5 | | Absolute max, current injected per pin |
| ESD_HBM | Electrostatic discharge human body model (ESD HBM) | – | | 2000 | V | All pins |
| ESD_CDM | Electrostatic discharge charged device model (ESD CDM) | | | 500 | | Charged device model ESD |
| LU | Pin current for latch-up | –100 | | 100 | mA | – |
| TJ | Junction temperature | –40 | | 125 | °C | |

**Note**

1. Usage above the absolute maximum conditions listed in **Table 4** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 5 Pin based absolute maximum ratings**

| Pin# | Pin name | Absolute minimum (V) | Absolute maximum (V) |
|---|---|---|---|
| 1 | SW1_0 | –0.7 | 35 |
| 2 | LG1_0[2] | –0.5 | PVDD + 0.5 |
| 3 | PGND_0 | –0.3 | 0.3 |
| 4 | PVDD_0 | | VDDD |
| 5 | LG2_0[2] | –0.5 | PVDD + 0.5 |
| 6 | VOUT_0 | –0.3 | 24 |
| 7 | SW2_0 | | 24 |
| 8 | HG2_0 (wrt SW2_0)[2] | –0.5 | PVDD + 0.5 |
| 9 | BST2_0 (wrt SW2_0)[2] | | |
| 10 | COMP_0[2] | –0.5 | |
| 11 | CSPO_0 | –0.3 | 24 |
| 12 | CSNO_0 | | |
| 13 | VBUS_IN_0 | | |
| 14 | VBUS_C_0 | | |
| 15 | CC1_0 | –0.5 | |
| 16 | CC2_0 | | |
| 17 | VBUS_CTRL_0 | | 32 |
| 18 | CSN_0_GPIO0[2] | | PVDD + 0.5 |
| 19 | CSP_0_GPIO1[2] | | |
| 20 | GPIO2[2] | | |
| 21 | GPIO3[2] | | |
| 22 | GPIO4[2] | | |
| 23 | DP_0_GPIO5[2] | | |
| 24 | DM_0_GPIO6[2] | | |
| 25 | VDDD | – | 6 |
| 26 | DM_1_GPIO7[2] | –0.5 | PVDD + 0.5 |
| 27 | DP_1_GPIO8[2] | | |
| 28 | XRES[2] | | |
| 29 | GPIO9[2] | | |
| 30 | GPIO10[2] | | |
| 31 | GPIO11[2] | | |
| 32 | CSP_1_GPIO12[2] | | |
| 33 | CSN_1_GPIO13[2] | | |
| 34 | GND | – | – |

**Notes**
2. Max voltage cannot exceed 6 V.
3. Max absolute voltage wrt GND must not exceed 40 V.

**Table 5 Pin based absolute maximum ratings** *(continued)*

| Pin# | Pin name | Absolute minimum (V) | Absolute maximum (V) |
|---|---|---|---|
| 35 | VBUS_CTRL_1 | –0.5 | 32 |
| 36 | CC2_1 | | 24 |
| 37 | CC1_1 | | |
| 38 | VBUS_C_1 | –0.3 | |
| 39 | VBUS_IN_1 | | |
| 40 | CSNO_1 | | |
| 41 | CSPO_1 | | |
| 42 | COMP_1[2] | –0.5 | PVDD + 0.5 |
| 43 | BST2_1[2] (wrt SW2_1) | | |
| 44 | HG2_1[2] (wrt SW2_1) | –0.5 | |
| 45 | SW2_1 | –0.3 | 24 |
| 46 | VOUT_1 | –0.3 | 24 |
| 47 | LG2_1[2] | –0.5 | PVDD + 0.5 |
| 48 | PVDD_1 | | VDDD |
| 49 | PGND_1 | –0.3 | 0.3 |
| 50 | LG1_1[2] | –0.5 | PVDD + 0.5 |
| 51 | SW1_1 | –0.7 | 35 |
| 52 | HG1_1[2, 3](wrt SW1_1) | –0.5 | PVDD + 0.5 |
| 53 | BST1_1[2, 3] (wrt SW1_1) | | |
| 54 | CSNI_1 | –0.3 | 40 |
| 55 | CSPI_1 | | 40 |
| 56 | GPIO14/SWD_DAT[2] | –0.5 | PVDD + 0.5 |
| 57 | GPIO15/SWD_CLK[2] | | |
| 58 | GPIO16[2] | | |
| 59 | GPIO17[2] | | |
| 60 | GPIO18[2] | | |
| 61 | VIN | –0.3 | 40 |
| 62 | VCCD | – | – |
| 63 | VDDD | | 6 |
| 64 | GND | | – |
| 65 | CSPI_0 | –0.3 | 40 |
| 66 | CSNI_0 | | |
| 67 | BST1_0[2, 3] (wrt SW1_0) | – | PVDD + 0.5 |
| 68 | HG1_0[2, 3] (wrt SW1_0) | –0.5 | |
| | EPAD | – | – |

**Notes**
2. Max voltage cannot exceed 6 V.
3. Max absolute voltage wrt GND must not exceed 40 V.

## 6.2 Device-level specifications

All specifications are valid for –40°C ≤ $T_A$ ≤ 105°C and $T_J$ ≤ 125°C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

### 6.2.1 DC specifications

**Table 6 DC specifications (operating conditions)**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.PWR#1 | VIN | Input supply voltage | 4.0 | – | 24 | V | – |
| SID.PWR#1A | VIN_BB | Buck Boost Operating input supply voltage | 5.5 | | 24 | | |
| SID.PWR#2 | VDDD_REG | VDDD output with VIN 5.5 V to 24 V, Max load = 150 mA | 4.6 | | 5.5 | | |
| SID.PWR#3 | VDDD_MIN | VDDD output with VIN 4 V to 5.5 V, Max load = 20mA | $V_{IN}$ – 0.2 | | – | | |
| SID.PWR#20 | VBUS | VBUS_C_0/1 valid range | 3.3 | | 21.5 | | |
| SID.PWR#5 | VCCD | Regulated output voltage (for Core Logic) | – | 1.8 | – | | |
| SID.PWR#16 | CEFC_VCCD | External regulator voltage bypass for VCCD | 80 | 100 | 120 | nF | X5R ceramic |
| SID.PWR#17 | CEXC_VDDD | Power Supply decoupling capacitor for VDDD | – | 10 | – | µF | |
| SID.PWR#18 | CEXV | Bootstrap supply capacitor (BST1_0, BST1_1, BST2_0, BST2_1) | | 0.1 | | | |
| SID.PWR#24 | IDD_ACT | Supply current at 0.4 MHz switching frequency | | 85 | | mA | TA = 25°C, VIN = 12 V. CC IO in transmit or receive, no I/O sourcing current, no VCONN load current, CPU at 24 MHz, two PD ports active. Buck-boost converter ON, 3-nF gate driver capacitance. |

**Table 6 DC specifications (operating conditions)** *(continued)*

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| **Deepsleep mode** | | | | | | | |
| SID_DS1 | IDD_DS1 | VIN = 12 V. CC wakeup on, Type-C not connected | – | 110 | – | µA | Type-C not attached, CC enabled for wakeup. Rp connection should be enabled for both PD ports. TA = 25°C. All faults disabled. |
| SID_DS2 | IDD_DS2 | VIN = 12 V | | 50 | | | USB-PD disabled. Wake-up from GPIO. TA = 25°C. |
| SID_DS3 | IDD_DS3 | $V_{IN}$ = 12 V. CC wakeup on, Type-C not connected | – | 450 | – | µA | Type-C not attached, CC enabled for wakeup. Rp connection should be enabled for both PD ports. $T_A$ = 25°C. All faults disabled except VBAT-GND. |

### 6.2.2 CPU

**Table 7 CPU specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#4 | $F_{CPU}$ | CPU input frequency | – | – | 48 | MHz | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$ |
| SID.PWR#19 | $T_{DEEPSLEEP}$ | Wakeup from deepsleep mode | | 35 | – | µs | – |
| SYS.XRES#5 | $T_{XRES}$ | External reset pulse width | 5 | – | | | |

### 6.2.3 GPIO

**Table 8 GPIO DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.GIO#9 | $V_{IH\_CMOS}$ | Input voltage HIGH threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS input |
| SID.GIO#10 | $V_{IL\_CMOS}$ | Input voltage LOW threshold | – | | 0.3 × $V_{DDD}$ | | |
| SID.GIO#7 | $V_{OH\_3V}$ | Output voltage HIGH level | $V_{DDD}$ – 0.6 | | – | | $I_{OH}$ = –4 mA, –40°C ≤ $T_A$ ≤ +105°C |
| SID.GIO#8 | $V_{OL\_3V}$ | Output voltage LOW level | – | | 0.6 | | $I_{OL}$ = 10 mA, –40°C ≤ $T_A$ ≤ +105°C |
| SID.GIO#2 | Rpu | Pull-up resistor when enabled | 3.5 | 5.6 | 8.5 | kΩ | –40°C ≤ $T_A$ ≤ +105°C |
| SID.GIO#3 | Rpd | Pull-down resistor when enabled | | | | | |
| SID.GIO#4 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | +25°C $T_A$, 3-V $V_{DDD}$ |
| SID.GIO#5 | $C_{PIN\_A}$ | Max pin capacitance | | | 22 | pF | –40°C ≤ $T_A$ ≤ +105°C, Capacitance on DP, DM pins |
| SID.GIO#6 | $C_{PIN}$ | | | 3 | 7 | | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$, all other I/Os |
| SID.GIO#11 | $V_{IH\_TTL}$ | LVTTL input | 2.0 | – | – | V | –40°C to +105°C $T_A$ |
| SID.GIO#12 | $V_{IL\_TTL}$ | | – | | 0.8 | | |
| SID.GIO#13 | $V_{HYSTTL}$ | Input hysteresis, LVTTL, $V_{DDD}$ > 2.7 V | 100 | – | – | mV | $V_{DDD}$ > 2.7 V |
| SID.GIO#14 | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.1 × $V_{DDD}$ | | | | – |

**Table 9 GPIO AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.GIO#16 | $T_{RISEF}$ | Rise time in fast strong mode | 2 | – | 12 | ns | $C_{load}$ = 25 pF, –40°C ≤ $T_A$ ≤ +105°C |
| SID.GIO#17 | $T_{FALLF}$ | Fall time in fast strong mode | | | | | |
| SID.GIO#18 | $T_{RISES}$ | Rise time in slow strong mode | 10 | | 60 | | |
| SID.GIO#19 | $T_{FALLS}$ | Fall time in slow strong mode | | | | | |
| SID.GIO#20 | $F_{GPIO\_OUT1}$ | GPIO $F_{OUT}$; 3.0 V ≤ $V_{DDD}$ ≤ 5.5 V, fast strong mode | – | | 16 | MHz | |
| SID.GIO#21 | $F_{GPIO\_OUT2}$ | GPIO $F_{OUT}$; 3.0 V ≤ $V_{DDD}$ ≤ 5.5 V, slow strong mode. | | | 7 | | |
| SID.GIO#22 | $F_{GPIO\_IN}$ | GPIO input operating frequency; 3.0 V ≤ $V_{DDD}$ ≤ 5.5 V. | | | 16 | | –40°C ≤ $T_A$ ≤ +105°C |

**Table 10 GPIO OVT DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID.GPIO_20VT_GIO#4 | GPIO_20VT_I_LU | GPIO_20VT latch up current limits | –140 | – | 140 | mA | Max / Min current in to any input or output, pin-to-pin, pin-to-supply |
| SID.GPIO_20VT_GIO#5 | GPIO_20VT_RPU | GPIO_20VT Pull-up resistor value | 3.5 | | 8.5 | kΩ | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$ |
| SID.GPIO_20VT_GIO#6 | GPIO_20VT_RPD | GPIO_20VT Pull-down resistor value | | | | | |
| SID.GPIO_20VT_GIO#16 | GPIO_20VT_IIL | GPIO_20VT Input leakage current (absolute value) | – | | 2 | nA | +25°C $T_A$, 3-V $V_{DDD}$ |
| SID.GPIO_20VT_GIO#17 | GPIO_20VT_CPIN | GPIO_20VT pin capaci-tance | | | 10 | pF | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$ |
| SID.GPIO_20VT_GIO#33 | GPIO_20VT_Voh | GPIO_20VT Output voltage high level. | VDDD – 0.6 | | – | V | $I_{OH}$ = -4 mA |
| SID.GPIO_20VT_GIO#36 | GPIO_20VT_Vol | GPIO_20VT Output Voltage low level. | – | | 0.6 | | $I_{OL}$ = 8 mA |
| SID.GPIO_20VT_GIO#41 | GPIO_20VT_Vih_LVTTL | GPIO_20VT LVTTL input | 2 | | – | | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$ |
| SID.GPIO_20VT_GIO#42 | GPIO_20VT_Vil_LVTTL | GPIO_20VT LVTTL input | – | | 0.8 | | |
| SID.GPIO_20VT_GIO#43 | GPIO_20VT_Vhysttl | GPIO_20VT Input hysteresis LVTTL | 100 | – | – | mV | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$ |
| SID.GPIO_20VT_GIO#45 | GPIO_20VT_ITOT_GPIO | GPIO_20VT Maximum total sink pin current to ground | – | | 95 | mA | V (GPIO_20VT pin) > $V_{DDD}$ |

**Table 11 GPIO OVT AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID.GPIO_20VT_70 | GPIO_20VT_TriseF | GPIO_20VT rise time in fast strong mode | 1 | – | 15 | ns | All $V_{DDD}$, $C_{load}$ = 25 pF |
| SID.GPIO_20VT_71 | GPIO_20VT_TfallF | GPIO_20VT fall time in fast strong mode | | | | | |
| SID.GPIO_20VT_GIO#46 | GPIO_20VT_TriseS | GPIO_20VT rise time in slow strong mode | 10 | | 70 | | |
| SID.GPIO_20VT_GIO#47 | GPIO_20VT_TfallS | GPIO_20VT fall time in slow strong mode | | | | | |
| SID.GPIO_20VT_GIO#48 | GPIO_20VT_FGPIO_OUT1 | GPIO_20VT GPIO Fout; 3 V ≤ $V_{DDD}$ ≤ 5.5 V. Fast strong mode. | – | | 33 | MHz | |
| SID.GPIO_20VT_GIO#50 | GPIO_20VT_FGPIO_OUT3 | GPIO_20VT GPIO Fout; 3 V ≤ $V_{DDD}$ ≤ 5.5V. Slow strong mode. | | | 7 | | |
| SID.GPIO_20VT_GIO#52 | GPIO_20VT_FGPIO_IN | GPIO_20VT GPIO input operating frequency; 3 V ≤ $V_{DDD}$ ≤ 5.5 V | | | 8 | | All $V_{DDD}$ |

## 6.2.4 XRES

**Table 12 XRES DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---|---|---|---|---|---|---|---|
| SID.XRES#1 | $V_{IH\_XRES}$ | Input voltage HIGH threshold on XRES pin | 0.7 × $V_{DDD}$ | – | – | V | CMOS input |
| SID.XRES#2 | $V_{IL\_XRES}$ | Input voltage LOW threshold on XRES pin | – | | 0.3 × $V_{DDD}$ | | |
| SID.XRES#3 | $C_{IN\_XRES}$ | Input capacitance on XRES pin | | | 7 | pF | – |
| SID.XRES#4 | $V_{HYSXRES}$ | Input voltage hysteresis on XRES pin | | 0.05 × $V_{DDD}$ | – | mV | |

## 6.3 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

### 6.3.1 Pulse-width modulation (PWM) for GPIO pins

**Table 13 PWM AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.1 | $TCPWM_{FREQ}$ | Operating frequency | – | – | Fc | MHz | Fc max = CLK_SYS |
| SID.TCPWM.3 | $T_{PWMEXT}$ | Output trigger pulse width | 2/Fc | | – | ns | Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs |
| SID.TCPWM.4 | $T_{CRES}$ | Resolution of counter | 1/Fc | | | | Minimum time between successive counts |
| SID.TCPWM.5 | $PWM_{RES}$ | PWM resolution | | | | | Minimum pulse width of PWM output |

### 6.3.2 $I^2C$

**Table 14 Fixed $I^2C$ AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Mbps | – |

### 6.3.3 UART

**Table 15 Fixed UART AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

### 6.3.4 SPI

**Table 16 Fixed SPI AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID166 | $F_{SPI}$ | SPI operating frequency (Master; 6X oversampling) | – | – | 8 | MHz | – |

**Table 17 Fixed SPI slave mode AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID170 | $T_{DMI}$ | MOSI valid before Sclock capturing edge | 40 | – | – | ns | – |
| SID171 | $T_{DSO}$ | MISO valid after Sclock driving edge | – | | $48 + (3 \times T_{CPU})$ | | $T_{CPU} = 1/F_{CPU}$ |
| SID171A | $T_{DSO\_EXT}$ | MISO valid after Sclock driving edge in Ext Clk mode | | | 48 | | – |
| SID172 | $T_{HSO}$ | Previous MISO data hold time | 0 | | – | | |
| SID172A | $T_{SSELSCK}$ | SSEL valid to first SCK valid edge | 100 | | | | |

**Table 18 Fixed SPI master mode AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID167 | $T_{DMO}$ | MOSI valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | $T_{DSI}$ | MISO valid before SClock capturing edge | 20 | | – | | Full clock, late MISO sampling |
| SID169 | $T_{HMO}$ | Previous MOSI data hold time | 0 | | | | Referred to slave capturing edge |

### 6.3.5 Memory

**Table 19 Flash AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.MEM#2 | FLASH_WRITE | Row (block) write time (erase and program) | – | – | 20 | ms | –40°C ≤ $T_A$ ≤ +85°C, All $V_{DDD}$ |
| SID.MEM#1 | FLASH_ERASE | Row erase time | | | 15.5 | | |
| SID.MEM#5 | FLASH_ROW_PGM | Row program time after erase | | | 7 | | |
| SID178 | $T_{BULKERASE}$ | Bulk erase time (32 KB) | | | 35 | | – |
| SID180 | $T_{DEVPROG}$ | Total device program time | | | 7.5 | s | |
| SID.MEM#6 | $FLASH_{ENPB}$ | Flash write endurance | 100k | | – | cycles | 25°C ≤ $T_A$ ≤ 55°C, All $V_{DDD}$ |
| SID182 | $F_{RET1}$ | Flash retention, $T_A$ ≤ 55°C, 100K P/E cycles | 20 | | | years | – |
| SID182A | $F_{RET2}$ | Flash retention, $T_A$ ≤ 85°C, 10K P/E cycles | 10 | | | | |

## 6.4 System resources

### 6.4.1 Power-on-reset (POR) with brown-out

**Table 20 Imprecise power-on reset (IPOR)**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID185 | $V_{RISEIPOR}$ | POR Rising trip voltage | 0.80 | – | 1.50 | V | –40°C ≤$T_A$ ≤ +105°C, All $V_{DDD}$. |
| SID186 | $V_{FALLIPOR}$ | POR Falling trip voltage | 0.70 | | 1.4 | | |

**Table 21 Precise POR**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID190 | $V_{FALLPPOR}$ | Brown-out detect (BOD) trip voltage in Active/Sleep modes | 1.48 | – | 1.62 | V | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$. |
| SID192 | $V_{FALLDPSLP}$ | BOD trip voltage in deepsleep mode | 1.1 | | 1.5 | | |

### 6.4.2 SWD interface

**Table 22 SWD interface specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.SWD#1 | F_SWDCLK1 | 3.0 V ≤ $V_{DDIO}$ ≤ 5.5 V | – | – | 14 | MHz | – |
| SID.SWD#2 | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25 × T | | – | ns | |
| SID.SWD#3 | T_SWDI_HOLD | | | | | | |
| SID.SWD#4 | T_SWDO_VALID | | – | | 0.50 × T | | |
| SID.SWD#5 | T_SWDO_HOLD | | 1 | | – | | |

### 6.4.3 Internal main oscillator

**Table 23 IMO AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#13 | $F_{IMOTOL}$ | Frequency variation at 48 MHz (trimmed) | – | – | ±2 | % | 3.0 V ≤ $V_{DDD}$ < 5.5 V. –40°C ≤ $T_A$ ≤ 105°C. |
| SID226 | $T_{STARTIMO}$ | IMO start-up time | | | 7 | µs | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$. |
| SID.CLK#1 | $F_{IMO}$ | IMO frequency | 24 | | 48 | MHz | |

### 6.4.4 Internal low-speed oscillator

**Table 24 ILO AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID234 | $T_{STARTILO1}$ | ILO start-up time | – | – | 2 | ms | –40°C ≤ $T_A$ ≤ +105°C, All $V_{DDD}$. |
| SID238 | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | |
| SID.CLK#5 | $F_{ILO}$ | ILO frequency | 20 | 40 | 80 | kHz | – |

### 6.4.5 PD

**Table 25 PD DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.DC.cc_shvt.1 | vSwing | Transmitter output high voltage | 1.05 | – | 1.2 | V | – |
| SID.DC.cc_shvt.2 | vSwing_low | Transmitter output low voltage | – | | 0.075 | | |
| SID.DC.cc_shvt.3 | zDriver | Transmitter output impedance | 33 | | 75 | Ω | |
| SID.DC.cc_shvt.4 | zBmcRx | Receiver input impedance | 10 | | – | MΩ | |
| SID.DC.cc_shvt.5 | Idac_std | Source current for USB standard advertisement | 64 | | 96 | µA | |
| SID.DC.cc_shvt.6 | Idac_1p5a | Source current for 1.5 A at 5 V advertisement | 166 | | 194 | | |
| SID.DC.cc_shvt.7 | Idac_3a | Source current for 3 A at 5 V advertisement | 304 | | 356 | | |
| SID.DC.cc_shvt.8 | Rd | Pull down termination resistance when acting as UFP (upstream facing port) | 4.59 | | 5.61 | kΩ | |
| SID.DC.cc_shvt.10 | zOPEN | CC impedance to ground when disabled | 108 | | – | | |
| SID.DC.cc_shvt.11 | DFP_default_0p2 | CC voltages on DFP side-standard USB | 0.15 | | 0.25 | V | |
| SID.DC.cc_shvt.12 | DFP_1.5A_0p4 | CC voltages on DFP side-1.5 A | 0.35 | | 0.45 | | |
| SID.DC.cc_shvt.13 | DFP_3A_0p8 | CC voltages on DFP side-3 A | 0.75 | | 0.85 | | |
| SID.DC.cc_shvt.14 | DFP_3A_2p6 | CC voltages on DFP side-3 A | 2.45 | | 2.75 | V | |
| SID.DC.cc_shvt.15 | UFP_default_0p66 | CC voltages on UFP side-standard USB | 0.61 | | 0.7 | | |
| SID.DC.cc_shvt.16 | UFP_1.5A_1p23 | CC voltages on UFP side-1.5 A | 1.16 | | 1.31 | | |
| SID.DC.cc_shvt.17 | Vattach_ds | Deepsleep attach threshold | 0.3 | | 0.6 | % | |
| SID.DC.cc_shvt.18 | Rattach_ds | Deepsleep pull-up resistor | 10 | | 50 | kΩ | |
| SID.DC.cc_shvt.19 | VTX_step | TX Drive voltage step size | 80 | | 120 | mV | |

### 6.4.6 Analog-to-digital converter

**Table 26 ADC DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.ADC.1 | Resolution | ADC resolution | – | 8 | – | Bits | – |
| SID.ADC.2 | INL | Integral non-linearity | –1.5 | – | 1.5 | LSB | Reference voltage generated from bandgap |
| SID.ADC.3 | DNL | Differential non-linearity | –2.5 | | 2.5 | | Reference voltage generated from $V_{DDD}$ |
| SID.ADC.4 | Gain Error | Gain error | –1.5 | | 1.5 | | Reference voltage generated from bandgap |
| SID.ADC.5 | VREF_ADC1 | Reference voltage of ADC | $V_{DDDmin}$ | | $V_{DDDmax}$ | V | Reference voltage generated from $V_{DDD}$ |
| SID.ADC.6 | VREF_ADC2 | Reference voltage of ADC | 1.96 | 2.0 | 2.04 | | Reference voltage generated from deepsleep reference |

## 6.4.7 HS CSA

**Table 27 HS CSA DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.HSCSA.1 | Csa_Acc1 | CSA accuracy<br>5 mV < Vsense < 10 mV | –15 | – | 15 | % | Active mode |
| SID.HSCSA.2 | Csa_Acc2 | CSA accuracy<br>10 mV < Vsense < 15 mV | –10 | | 10 | | |
| SID.HSCSA.3 | Csa_Acc3 | CSA accuracy<br>15 mV < Vsense < 25 mV | –5 | | 5 | | |
| SID.HSCSA.4 | Csa_Acc4 | CSA accuracy<br>25 mV < Vsense | –3 | | 3 | | |
| SID.HSCSA.7 | Csa_SCP_Acc1 | CSA SCP at 6 A with 5-mΩ sense resistor | –10 | | 10 | | |
| SID.HSCSA.8 | Csa_SCP_Acc2 | CSA SCP at 10 A with 5-mΩ sense resistor | | | | | |
| SID.HSCSA.9 | Csa_OCP_1A | CSA OCP at 1 A with 5-mΩ sense resistor | 104 | 130 | 156 | | |
| SID.HSCSA.10 | Csa_OCP_5A | CSA OCP for 5 A with 5-mΩ sense resistor | 123 | 130 | 137 | | |

**Table 28 HS CSA AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.HSCSA.AC.1 | $T_{SCP\_GATE}$ | Delay from SCP threshold trip to external NFET power gate turn off | – | 3.5 | – | µs | 1-nF NFET gate |
| SID.HSCSA.AC.2 | $T_{SCP\_GATE\_1}$ | Delay from SCP threshold trip to external NFET power gate turn off | | 8 | | | 3-nF NFET gate |

## 6.4.8 UV/OV

**Table 29 UV/OV specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.UVOV.1 | $V_{THOV1}$ | Overvoltage threshold Accuracy, 4 V to 11 V | –3 | – | 3 | % | Active mode |
| SID.UVOV.2 | $V_{THOV2}$ | Overvoltage threshold Accuracy, 11 V to 21.5 V | –3.2 | | 3.2 | | |
| SID.UVOV.3 | $V_{THUV1}$ | Undervoltage threshold Accuracy, 3 V to 3.3 V | –4 | | 4 | | |
| SID.UVOV.4 | $V_{THUV2}$ | Undervoltage threshold Accuracy, 3.3 V to 4.0 V | –3.5 | | 3.5 | | |
| SID.UVOV.5 | $V_{THUV3}$ | Undervoltage threshold Accuracy, 4.0 V to 21.5 V | –3 | | 3 | | |

### 6.4.9 VCONN switch

**Table 30 VCONN switch DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| DC.VCONN.1 | VCONN_OUT | VCONN output voltage with 20 mA load current | 4.5 | – | 5.5 | V | – |
| DC.VCONN.2 | $I_{LEAK}$ | Connector side pin leakage current | – | | 10 | µA | |
| DC.VCONN.3 | $I_{OCP}$ | VCONN over-current protection threshold | 22.5 | 30 | 37.5 | mA | |

**Table 31 VCONN switch AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| AC.VCONN.1 | $T_{ON}$ | VCONN switch turn-on time | – | – | 600 | µs | – |
| AC.VCONN.2 | $T_{OFF}$ | VCONN switch turn-off time | | | 10 | | |

### 6.4.10 $V_{BUS}$

**Table 32 $V_{BUS}$ discharge specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.VBUS.DISC.1 | R1 | 20-V NMOS ON resistance for DS = 1 | 500 | – | 2000 | Ω | Measured at 0.5 V |
| SID.VBUS.DISC.2 | R2 | 20-V NMOS ON resistance for DS = 2 | 250 | | 1000 | | |
| SID.VBUS.DISC.3 | R4 | 20-V NMOS ON resistance for DS = 4 | 125 | | 500 | | |
| SID.VBUS.DISC.4 | R8 | 20-V NMOS ON resistance for DS = 8 | 62.5 | | 250 | | |
| SID.VBUS.DISC.5 | R16 | 20-V NMOS ON resistance for DS = 16 | 31.25 | | 125 | | |
| SID.VBUS.DISC.6 | Vbus_stop_error | Error percentage of final VBUS value from setting | – | | 10 | % | When VBUS is discharged to 5 V |

### 6.4.11 Voltage regulation

**Table 33 Voltage regulation DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.DC.VR.1 | VOUT | VBUS_IN output voltage range | 3.3 | – | 21.5 | V | – |
| SID.DC.VR.2 | VR | VBUS_IN voltage regulation accuracy | – | ±3 | ±5 | % | |
| SID.DC.VR.3 | VIN_UVLO | VIN Supply below which chip will get reset | 1.7 | – | 3.0 | V | |

**Table 34 Voltage regulator specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.VREG.1 | $T_{START}$ | Total startup time for the regulator supply outputs | – | – | 200 | µs | – |

### 6.4.12 VBUS gate driver

**Table 35 VBUS gate driver DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.GD.1 | GD_VGS | Gate to source overdrive during ON condition | 4.5 | 5 | 10 | V | NFET driver is ON |
| SID.GD.2 | GD_RPD | Resistance when pull-down enabled | – | – | 2 | kΩ | Applicable on VBUS_CTRL to turn off external NFET |
| SID.GD.5 | GD_drv | Programmable typical gate current | 0.3 | | 9.75 | µA | – |

**Table 36 VBUS gate driver AC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.GD.3 | $T_{ON}$ | VBUS_CTRL LOW to HIGH (1 V to VBUS + 1 V) with 3-nF external capacitance | 2 | 5 | 10 | ms | $V_{BUS\_IN}$ = 5 V |
| SID.GD.4 | $T_{OFF}$ | VBUS_CTRL HIGH to LOW (90% to 10%) with 3-nF external capacitance | – | 7 | – | µs | $V_{BUS\_IN}$ = 21.5 V |

#### 6.4.12.1 PWM controller

**Table 37 Buck-boost PWM controller specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| PWM.1 | $F_{SW}$ | Switching frequency | 150 | – | 600 | kHz | – |
| PWM.2 | FSS | Spread spectrum frequency dithering span | – | 10 | – | % | |
| PWM.3 | Ratio_Buck_BB | Buck to buck boost ratio | | 1.16 | | – | |
| PWM.4 | Ratio_Boost_BB | Boost to buck boost ratio | | 0.84 | | | |

### 6.4.12.2 NFET gate driver

**Table 38 Buck-boost NFET gate driver specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| DR.1 | R_HS_PU | Top-side gate driver on-resistance - Gate pull-up | – | 2 | – | Ω | – |
| DR.2 | R_HS_PD | Top-side gate driver on-resistance - Gate pull-down | | 1.5 | | | |
| DR.3 | R_LS_PU | Bottom-side gate driver on-resistance - Gate pull-up | | 2 | | | |
| DR.4 | R_LS_PD | Bottom-side gate driver on-resistance - Gate pull-down | | 1.5 | | | |
| DR.5 | Dead_HS | Dead time before high-side rising edge | | 30 | | ns | |
| DR.6 | Dead_LS | Dead time before low-side rising edge | | | | | |
| DR.7 | Tr_HS | Top-side gate driver rise time | | 25 | | | |
| DR.8 | Tf_HS | Top-side gate driver fall time | | 20 | | | |
| DR.9 | Tr_LS | Bottom-side gate driver rise time | | 25 | | | |
| DR.10 | Tf_LS | Bottom-side gate driver fall time | | 20 | | | |

### 6.4.12.3 LS-SCP

**Table 39 LS-SCP DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.LSSCP.DC.1 | SCP_6A | Short circuit current detect @ 6A | 5.4 | 6 | 6.6 | A | Using differential inputs (CSN_1_GPIO12, CSP_1_GPIO13 or CSP_0_GPIO0, CSN_0_GPIO1) |
| SID.LSSCP.DC.1A | SCP_6A_SE | Short circuit current detect @ 6A | 4.5 | 6 | 7.5 | | Using single ended inputs (CSP_1_GPIO13 or CSP_0_GPIO0) and internal ground |
| SID.LSSCP.DC.2 | SCP_10A | Short circuit current detect @10A | 9 | 10 | 11 | | Using differential inputs (CSN_1_GPIO12, CSP_1_GPIO13 or CSP_0_GPIO0, CSN_0_GPIO1) |
| SID.LSSCP.DC.2A | SCP_10A_SE | Short circuit current detect @10A | 7.5 | 10 | 12.5 | | Using single ended inputs (CSP_1_GPIO13 or CSP_0_GPIO0) and internal ground |

### 6.4.12.4 Thermal specifications

**Table 40 Thermal specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---|---|---|---|---|---|---|---|
| SID.OTP.1 | OTP | Thermal shutdown | 120 | 125 | 130 | °C | – |

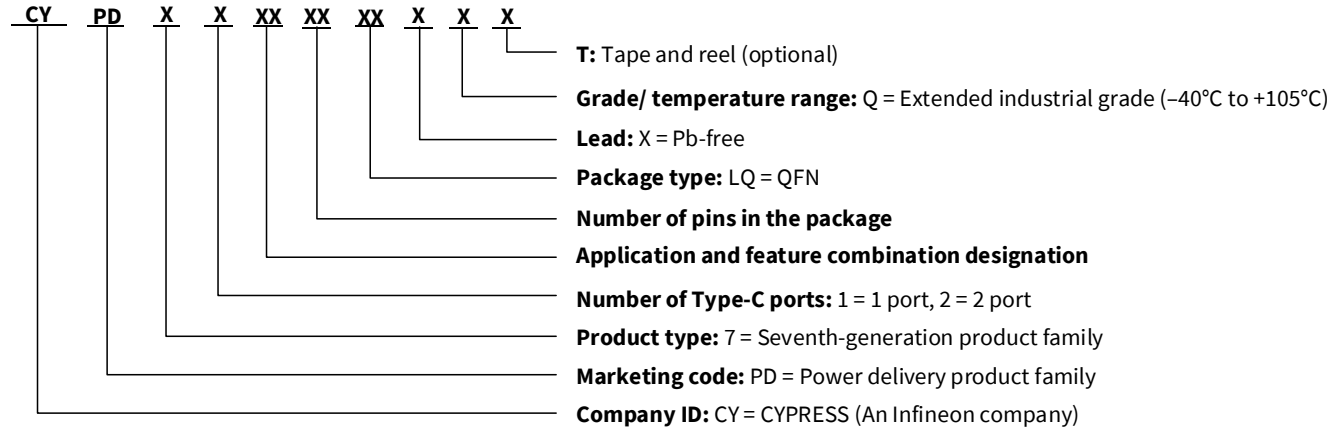
# 7 Ordering information

Table 41 lists the EZ-PD™ CCG7DC part numbers and features.

**Table 41 EZ-PD™ CCG7DC ordering information**

| MPN | Application | Bootloader | Termination resistor | Role | Switching frequency | Package type |
|---|---|---|---|---|---|---|
| CYPD7271-68LQXQ | Dual-port USB-C PD AC-DC power adapter/ cigarette lighter adapter (CLA) | PSoC™ Creator based Bootloader | $R_P$ | DFP (Power source only) | 150 kHz to 600 kHz | 68-pin QFN |
| CYPD7271-68LQXQT | | | | | | |
| CYPD7272-68LQXQ | Dual-port USB-C PD AC-DC power adapter/ cigarette lighter adapter (CLA)<br><br>Multi-port AC-DC charger and adapter | ModusToolbox™ based Bootloader | | | | |
| CYPD7272-68LQXQT | | | | | | |

## 7.1 Ordering code definitions



# 8 Packaging

**Table 42 Package characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_J$ | Operating junction temperature | – | –40 | 25 | 125 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ | | – | – | 14.8 | °C/W |
| $T_{JB}$ | Package $\theta_{JB}$ | | | | 4.3 | |
| $T_{JC}$ | Package $\theta_{JC}$ | | | | 12.9 | |

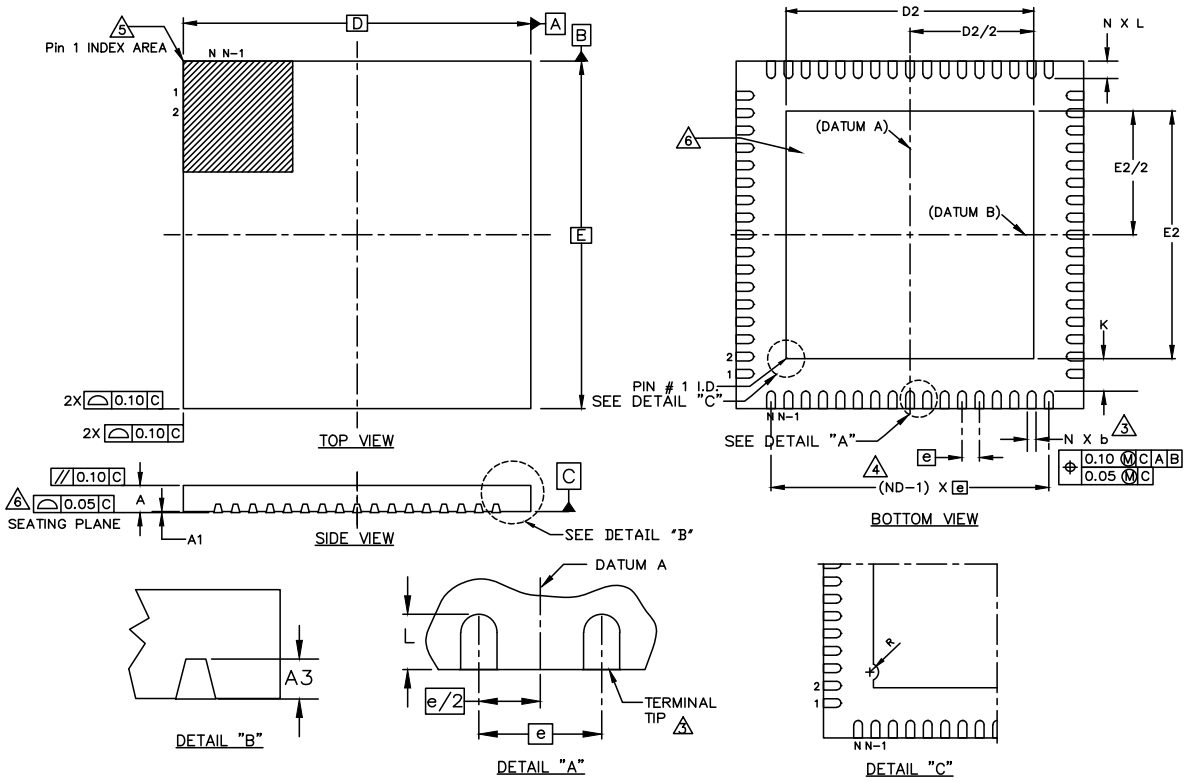
**Table 43 Solder reflow peak temperature**

| Package | Maximum peak temperature | Maximum time within 5°C of peak temperature |
|---|---|---|
| 68-pin QFN | 260°C | 30 seconds |

**Table 44 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 68-pin QFN | MSL 3 |

# 9 Package diagram




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| e | | 0.40 BSC | |
| N | | 68 | |
| ND | | 17 | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.15 | 0.20 | 0.25 |
| D2 | 5.60 | 5.70 | 5.80 |
| E2 | 5.60 | 5.70 | 5.80 |
| D | | 8.00 BSC | |
| E | | 8.00 BSC | |
| A | - | - | 0.65 |
| A1 | 0.00 | - | 0.05 |
| A3 | | 0.203 REF | |
| R | | 0.20 TYP | |
| K | | 0.75 MIN | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-31802 *D

**Figure 12 68-lead QFN ((8 × 8 × 0.65 mm) LD68B 5.7 × 5.7 mm E-Pad (Sawn)) package outline (PG-VQFN-68-800), 002-31802**

# 10 Acronyms

**Table 45 Acronyms used in this document**

| Acronym | Description |
|---|---|
| ADC | analog-to-digital converter |
| AFC | Samsung adaptive fast charging |
| Arm® | advanced RISC machine, a CPU architecture |
| CPU | central processing unit |
| CSA | current sense amplifier |
| DAC | digital-to-analog converter |
| FCCM | forced continuous current/conduction mode |
| GPIO | general-purpose input/output |
| HSDR | high-side driver |
| $I^2C$, or IIC | inter-integrated circuit, a communications protocol |
| IDAC | current DAC |
| I/O | input/output, see also GPIO |
| LSDR | low-side driver |
| MCU | microcontroller unit |
| OCP | overcurrent protection |
| OVP | overvoltage protection |
| PD | power delivery |
| POR | power-on reset |
| PSoC™ | Programmable system-on-chip |
| PSM | pulse skipping mode |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| SPI | serial peripheral interface, a communications protocol |
| SRAM | static random access memory |
| TCPWM | timer/counter/PWM |
| Type-C | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART | universal asynchronous transmitter receiver, a communications protocol |
| UFP | upstream facing port |
| UVP | undervoltage protection |
| USB | universal Serial Bus |
| UVLO | under-voltage lockout |
| ZCD | zero crossing detector |

# 11 Document conventions

## 11.1 Units of measure

**Table 46 Units of measure**

| Symbol | Unit of measure |
|---|---|
| °C | degrees Celsius |
| Hz | hertz |
| KB | 1024 bytes |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| mΩ | milliohm |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| W | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| *C | 2022-10-19 | Post to external web. |
| *D | 2023-01-16 | Updated **Electrical specifications**:<br>Updated **Device-level specifications**:<br>Updated **CPU**:<br>Updated **Table 7**.<br>Updated **Ordering information**:<br>Updated **Table 41** (Updated part numbers).<br>Updated to new template.<br>Completing Sunset Review. |
| *E | 2023-07-10 | Updated Document Title to read as “CYPD7271, CYPD7272, EZ-PD™ CCG7DC dual-port USB-C power delivery and DC-DC controller”.<br>Updated **Applications**:<br>Updated description.<br>Updated **Applications**:<br>Updated **Figure 10**.<br>Updated **Figure 11**.<br>Removed table “Multi-port AC-DC adapter GPIO pin mapping for application diagram in Figure 11”.<br>Updated **Ordering information**:<br>Updated **Table 41** (Updated part numbers).<br>Updated **Package diagram**:<br>spec 002-31802 – Changed revision from *C to *D. |

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