Recommendations for Board Assembly of Infineon Integrated Packages without Leads

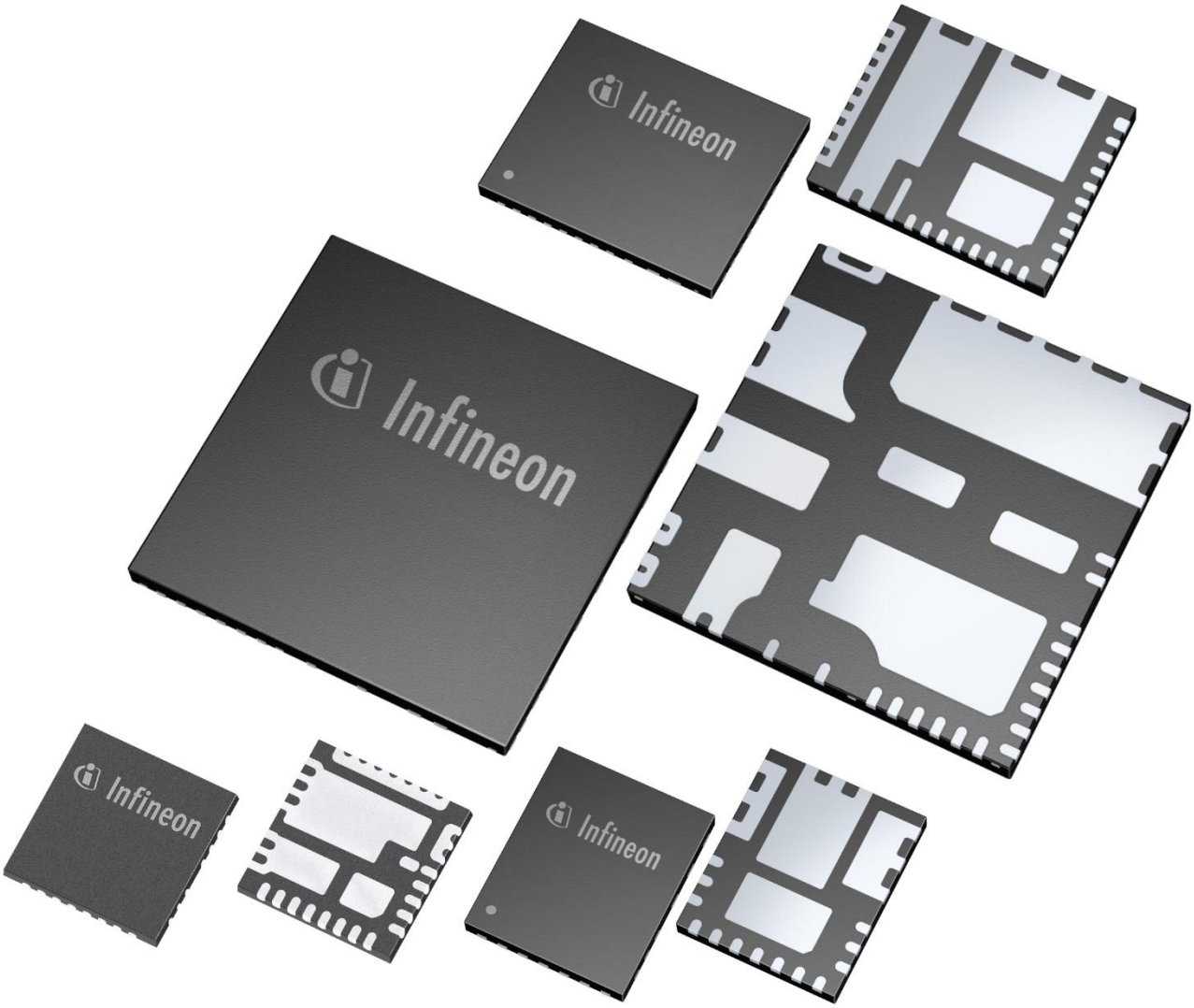

Table of Contents

Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
DFN	Dual-Flat No-Leads
ESD	Electrostatic Discharge
IQFN	Integrated Quad Flat No-Leads
MSL	Moisture-Sensitivity Level
NSMD	Non-Solder Mask Defined
PG	Plastic Green
PCB	Printed Circuit Board
PQFN	Power Quad Flat No-lead
QFN	Quad-Flat No-lead
SAC	Tin Silver Copper (SnAgCu)
SMD	Solder Mask Defined pad
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
Sn	matte tin plating
SON	Small Outline Non-leaded package
TISON	Thin-profile Integrated Small-Outline Non-leaded package
WISON	Very Very thin-profile Integrated Small-Outline Non-leaded

1 Package Description

This document provides information about the Surface Mount Technology (SMT) board assembly of integrated Quad Flat No-Lead packages (QFN) and integrated Small-Outline Non-leaded (SON) packages featuring low or no footprint symmetries. This document does not discuss discrete QFN or discrete SON packages including SON packages with redundant dies (dual-pad versions). These package families are described in separate documents.

The multi-chip packages discussed herein encapsulate two or more silicon dies. A resulting feature are multiple-segmented die pads for individual current flow while maintaining the necessary thermal management. Fused perimeter pads can form interconnected source leads which provide an extended path for heat dissipation and current flow preventing effects such as current crowding.

1.1 QFN Package Type

Infineon QFN packages with multiple integrated devices are represented by the Integrated Quad Flat No-Lead (IQFN) package family. Another designation can be Power Quad Flat No-Lead package (PQFN). **Figure 1** shows examples of the IQFN package family.

- PG-IQFN packages

PG = Plastic Green
I = Integrated
QFN = Quad Flat No-lead

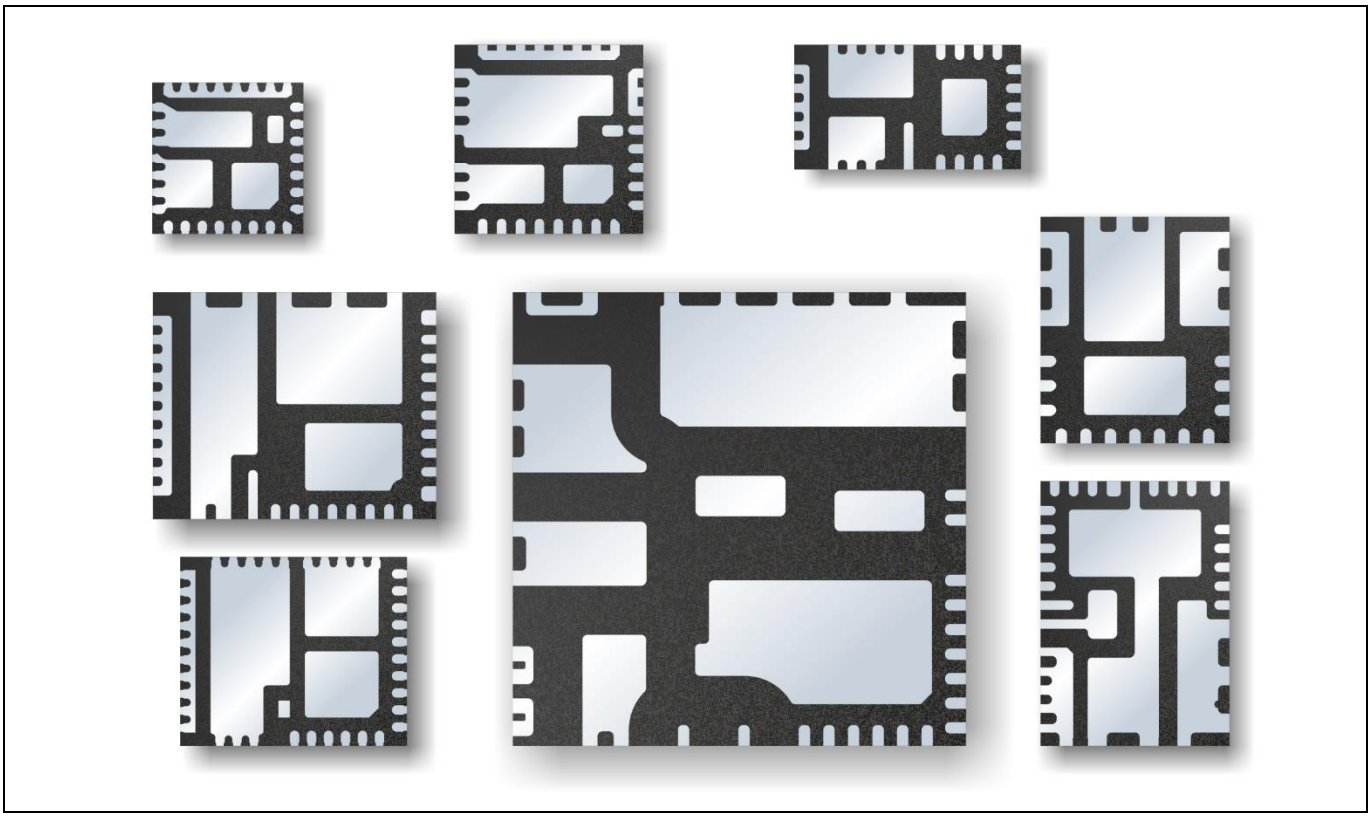

Figure 1 Examples of IQFN packages.

1.3 SON Package Type

Infineon integrated SON packages can be classified by thickness, and include Thin-profile Integrated Small-Outline Non-leaded (TISON) packages or Very Very thin-profile Integrated Small-Outline Non-leaded (WISON) packages. They often feature a higher degree of footprint symmetry compared to integrated QFN packages. Integrated SON packages can also be designated as PQFN or Dual Flat No-Lead (DFN) packages. **Figure 2** shows examples of the TISON and WISON package families.

- PG-TISON packages
- PG-WISON packages

PG = Plastic Green
T = Thin-profile
W = Very Very thin-profile
I = Integrated
SON = Small-Outline Non-leaded

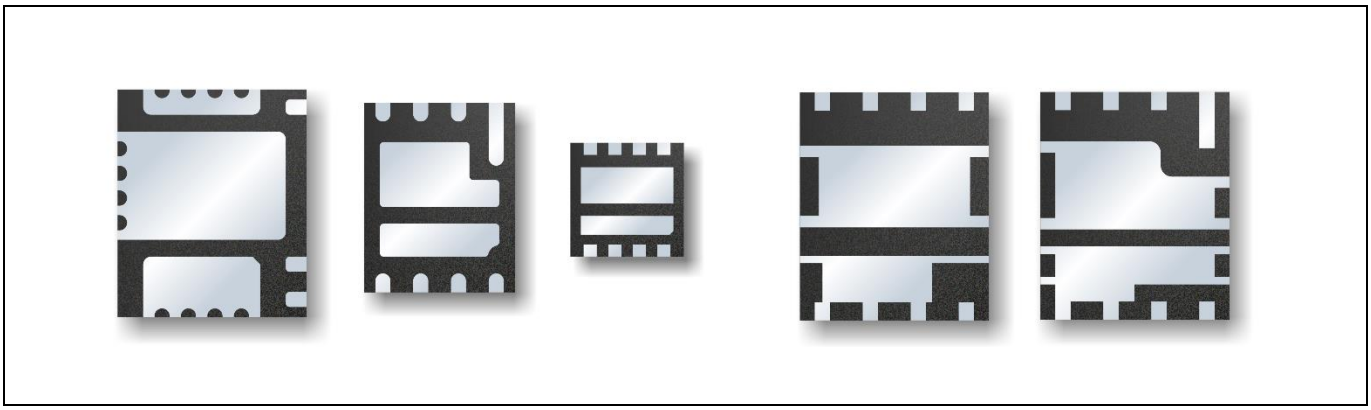

Figure 2 Examples of TISON and WISON packages.

1.4 Package Features and General Handling Guidelines

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal Construction

The components of the integrated QFN and SON package families feature multiple plastic-encapsulated chips on a copper leadframe using perimeter lands as well as segmented die-pads on the bottom to provide electrical and thermal contact to the Printed Circuit Board (PCB).

Depending on the thermal output produced by the dies, areas for heat transfer are provided by appropriately dimensioned exposed die pads.

The electrical connection between the die and the leadframe can be implemented in various ways as shown in **Figure 3**. Versions with copper clip interconnects provide an overall low conduction resistance due to the increased conductor cross-section.

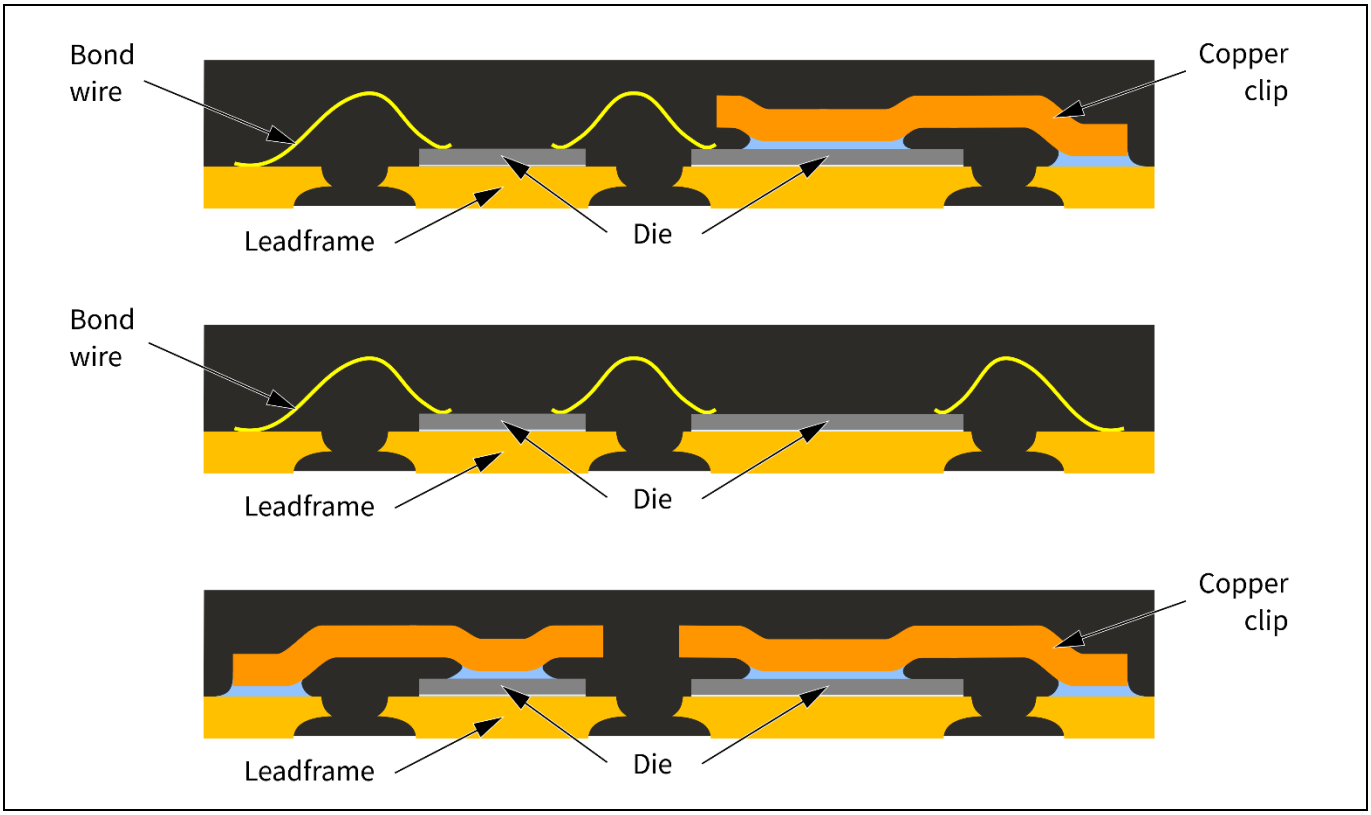

Figure 3 **Schematics showing the inner setups of a configuration with wire bonds and clips (top), with wire bonds only (center), and with clips only (bottom).**

Termination Design

The non-leaded land pattern provides for optimal electrical performance due to decreased conductor lengths, while optimizing the package-to-chip ratio.

The leadframe singulation of the integrated QFN and SON packages is created by sawing of array molded packages. The resulting termination flank can be seen in **Figure 4**. The solder joints are mainly formed underneath the package. The tips of such terminations often feature bare copper (e.g. cut edges) and are therefore not intended to wet with solder by design according to IPC-A-610 [6].

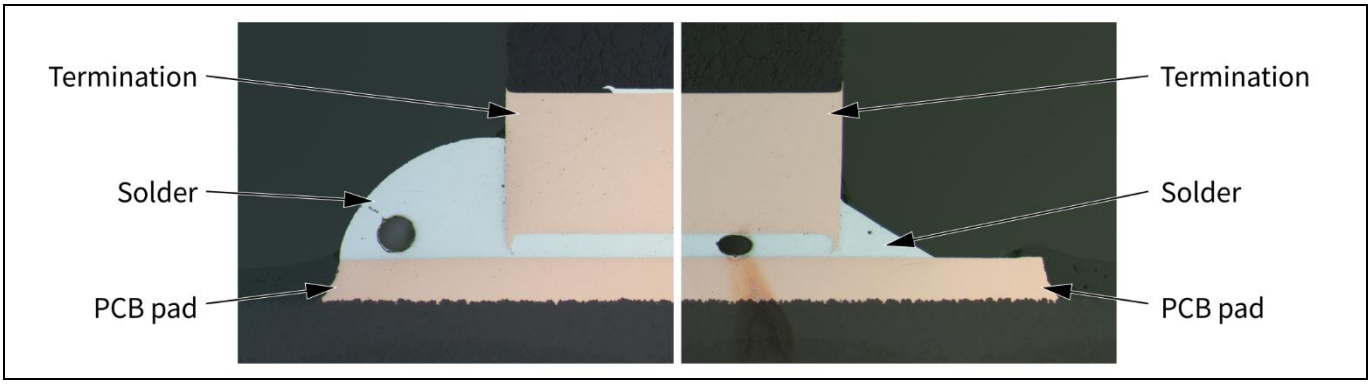

Figure 4 **Cross-sections of sawn map mold package terminations. The solder wetting height on the sidewall can be inconsistent with no negative impact on the component's performance.**

Termination Plating

Infineon QFP are available with matte tin (Sn) surface finish or with a Pre-Plated lead Frame (PPF). While the Sn plating is applied to the base metal by a post-mold process, the PPF provides a solderable surface that is already deposited on the lead frame prior to the die attach process. The PPF surfaces basically consist of a nickel/palladium/gold (Ni/Pd/Au) stack-up. While the Sn melts during reflow, the sacrificial Au layer of the PPF surface is dissolved. The solder connection is then made with the Ni layer.

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each other on either side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder-Mask Defined, SMD or Non-Solder-Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

Beside their electrical function, the exposed pads on the landing area of the integrated QFN and SON packages are designed to conduct high thermal loads into the PCB in order to achieve optimal thermal performance. Therefore, the exposed pad area on the PCB should be congruent with the area on the package.

For optimal heat dissipation in high-current applications, the SMD pad type is preferred since it allows for large copper areas under the solder mask layer of the PCB. Beside the power application aspect, the SMD design type can also be beneficial in terms of routing flexibility.

If the central die pad is not used as a thermal pad, it is still a connection to ground. Using a PCB pad of the same size as the package pad will also increase the solder joint reliability as well as the electrical performance for some applications. Two examples of SMD footprints are shown in **Figure 5**.

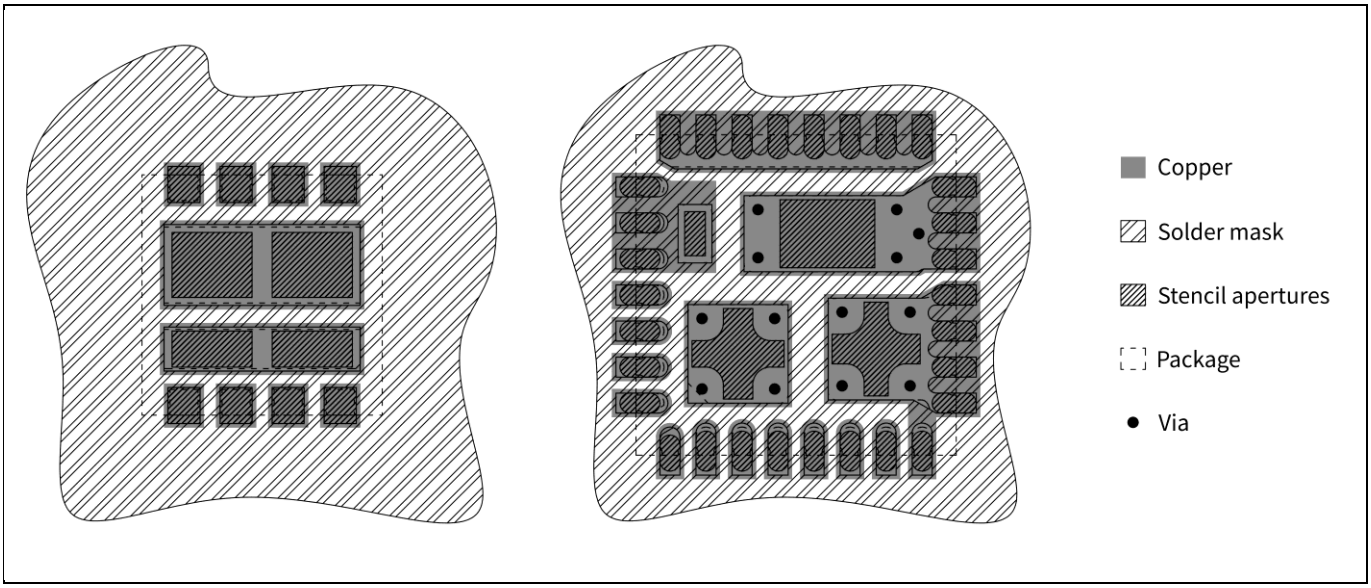

Figure 5 Example of SMD pads and stencil apertures for an integrated SON package (left) and with a potential via solution for an integrated QFN package (right).

Mixing different pad definition types in one footprint is not recommended. **Figure 6** shows the general approach for PCB pad design. The cut edges of the terminations are not intended to be wettable by design (see also IPC-A-610 [6]), which makes all terminations of the integrated QFN and SON components of the “bottom only” type. In order to support the self-aligning effect by the liquid solder wetting forces during reflow, it is recommended to extend the PCB pads by approx. 250 µm beyond the package perimeter and by approx. 50 µm in the heel region of the termination.

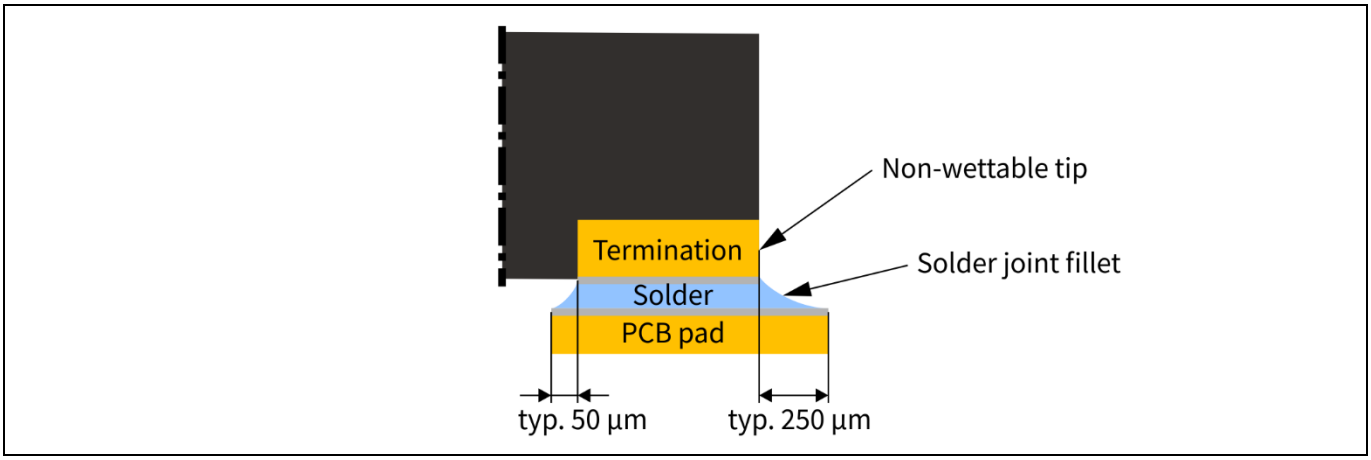

Figure 6 Schematic depiction of the perimeter pad design on the PCB and the expected solder fillet formation.

Generally, an optimal PCB design depends on the specific application as well as on the specific design guidelines of the chosen board manufacturer.

For further information about PCB pad design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

2.3 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat is then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization. The implementation of thermal vias has several impacts on the board assembly as outlined below. A constant increase of number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimum number of vias needed.

One of the primary exposed pad design objectives, besides the thermal management, should be to avoid the penetration of the vias by solder. Consequences of solder penetration can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area or surplus solder on the opposite side of the PCB.

A first approach for risk reduction should be the prevention of a direct print of solder paste on the via opening. Since the stencil for large area prints such as on die pads is usually segmented, it is a good practice to position

the vias under the beam intersections of the aperture as shown in **Figure 5**. With such an approach, a good solder joint on a central die pad can be formed using vias that remain open on both sides of the board.

Components with a non-centered die pad tend to tilt due to the varying solder volume along the package axis. Therefore, despite the precautionary stencil design approach, the solder can move into the via, driven by the wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, dummy areas on the opposite side as shown in **Figure 7** can catch the surplus solder to avoid beading and solder lumping.

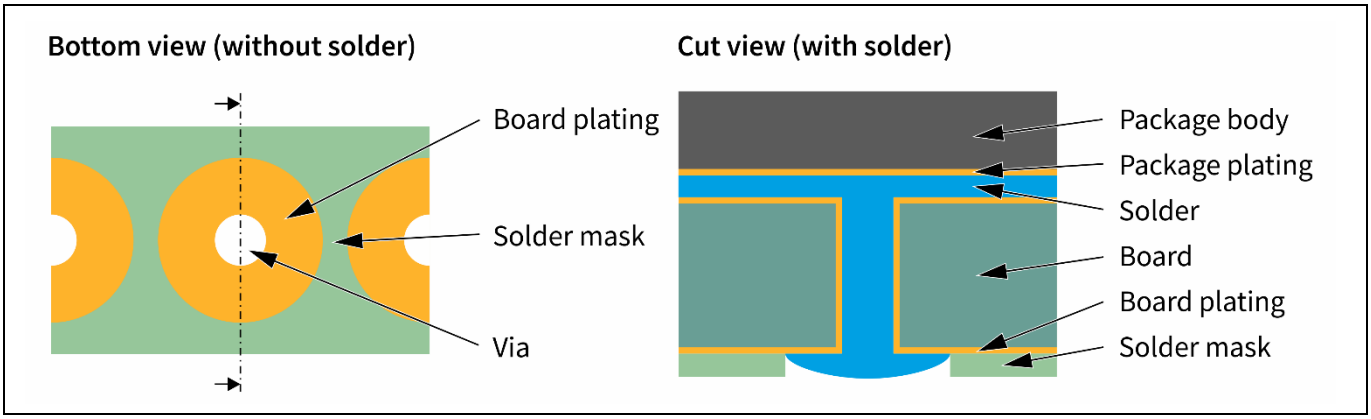

Figure 7 Wettable “dummy” area that surrounds the vias on the opposite side of the board to act as a buffer for surplus solder.

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by “tenting.” This process includes covering the vias by a solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in diameter or smaller) should be filled with copper and overplated. In both cases, the specification of a planar filling is necessary to avoid cavities that will trap gases, forming voids during reflow soldering.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias can be placed next to the footprint near the package and covered with solder mask.

For further information about vias in pad, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. The latter are applied especially when fine-pitch components are assembled.

In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical integrated QFN or SON packages, stencils with a thickness of 100 µm to 120 µm are recommended.

The solder paste volume in apertures larger than approximately 5 mm may be scooped out depending on the specific squeegee pressure and rigidity. Such apertures are necessary for many die pad prints and should be segmented into smaller areas. The reduction of the die pad print can also reduce the tilt of one-axis non symmetric components towards their leads side. Generally, for packages with a symmetric or near-symmetric footprint, the die pad print is reduced by 50% to 70%. When reducing the die pad print, potential vias in the pad can be considered as outlined in the relevant section above. However, when it comes to packages with no symmetry or only near-symmetry axis, individual designs based on a uniform solder distribution over all terminations should be used. The target solder joint stand-off should be between 40 µm and 60 µm.

For individual design adaptations to reach the optimum amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Using Type 3 or Type 4 paste is recommended for the assembly of integrated SON and QFN components, depending on the specific stencil aperture size and therefore solder paste transfer efficiency.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For leadless packages in which the solder joint is formed mainly on the package bottom side, a “no clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating. For

power packages, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminations and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For PCB assembly of the integrated QFN and SON components, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the solderability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

Infineon integrated QFN and SON packages are generally suited for mounting on double-sided PCBs. If the solder joint thickness is a critical dimension, solder joints of components on the first side will again reflow in the second step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held in place by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder

joints, unlike joints on the top side, where gravity will force the components closer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

For further information about reflow soldering, please refer to *the General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminations is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

Compared to leaded SMD components (e.g. the gullwing type), the solder joints of integrated QFN and SON packages are mainly formed underneath the package. **Figure 8** shows solder joint fillets of an IQFN component with SMD pad design. The tips of the terminations often have bare copper (cut or stamped edges) that are not designed to be wetted by solder according to IPC-A-610 [6]. Non-wetting of such termination tips is not a criterion for rejection. Consequently, reliable visual inspection of such solder joints with conventional Automated Optical Inspection (AOI) systems is limited.

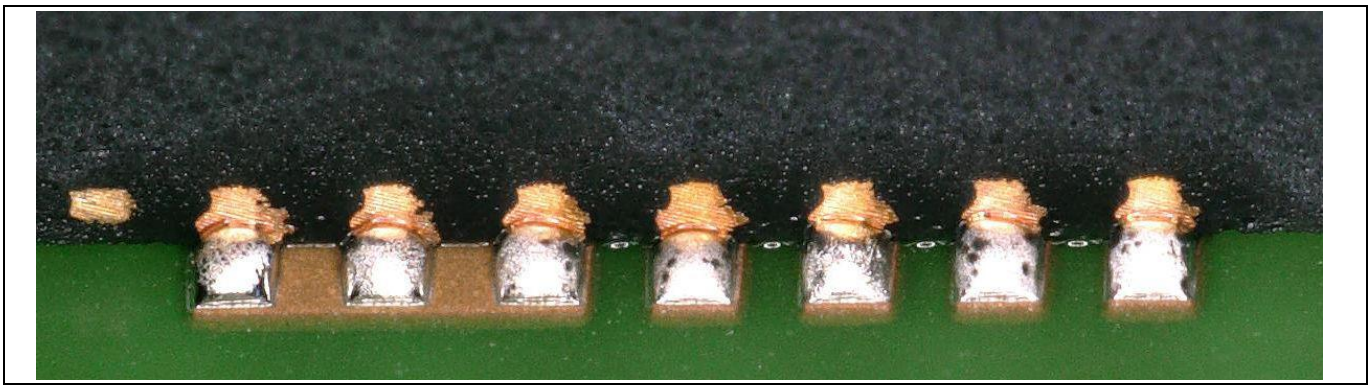

Figure 8 Photograph of a soldered IQFN package on SMD PCB pads.

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of components that cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 9 shows a typical X-ray photograph of a dummy IQFN component (without internal setup such as chip, clip, or wire bond) after board assembly. The leadframe and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increase voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the board pad size, the stencil layout, the solder paste, the reflow profile, and the via layout. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

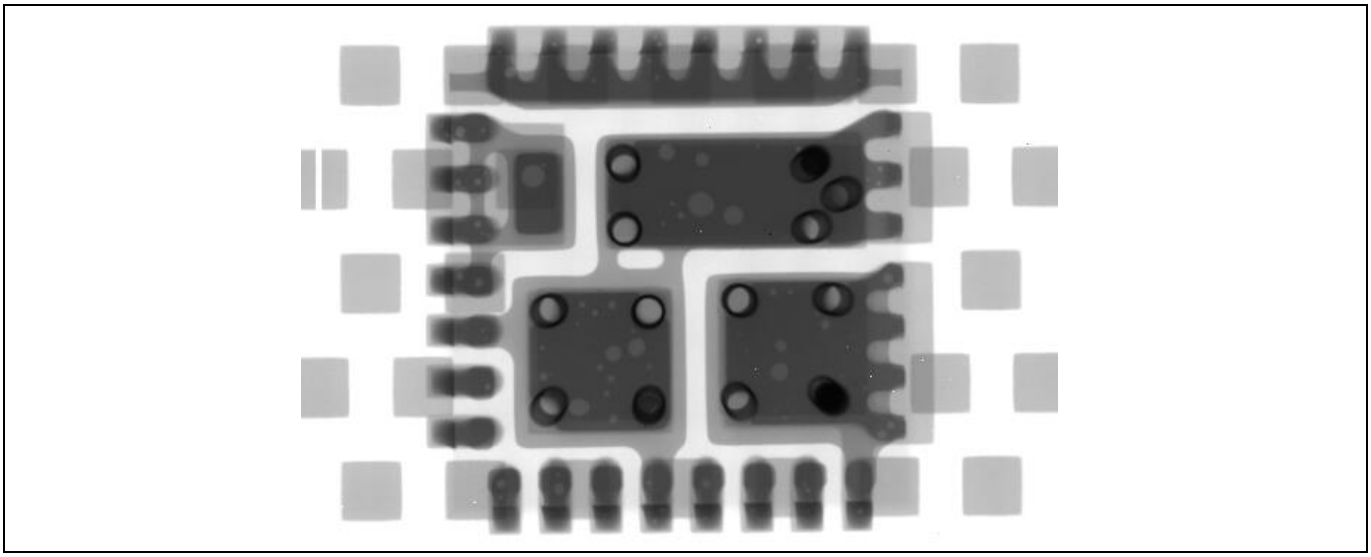

Figure 9 **Typical X-ray image of a soldered IQFN package. Investigations have shown that voids similar in size and amount to those shown in this image do not reduce the package reliability.**

6 Rework

Single solder joint repair of bottom-only terminated packages is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (i.e. onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 6 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-12-18

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.