CoolSiC™ MOSFET M1H for modules - Application Note

About this document

Scope and purpose

The benefits of wide-bandgap silicon carbide (SiC) semiconductors arise from their higher breakthrough electric field, larger thermal conductivity, higher electron-saturation velocity and lower intrinsic carrier concentration compared to silicon (Si). Based on these SiC material advantages, SiC MOSFETs are an attractive switching transistor for high-power applications, such as solar inverters, off- & on-board electric vehicles (EV) chargers.

This application note introduces the CoolSiC™ trench MOSFET M1H technology for modules, describing the general features and characteristics of CoolSiC™ MOSFET's M1H generation, which can help in designing power systems effectively using the novel transistor.

Intended audience

This application note is intended for development, design- and qualification engineers working with CoolSiC™ MOSFET M1H modules.

Table of contents

1 Infineon 1200 V SiC Trench CoolSiC™ MOSFET M1H

The CoolSiC™ MOSFET M1H is the successor of the CoolSiC™ MOSFET M1 available today, and brings significant advantages for the applications. In the following we highlight some of the main features and benefits:

- On-state resistance $R_{DS(on)}$:
  The CoolSiC™ MOSFET 1200V M1H shows compared to the generation M1 a 12% reduced $R_{DS(on)}$ at an application relevant temperature of $T_{vj\,op}$ = 125 °C and $V_{GS(on)}$ = 18V
- Gate-source voltage:
  The CoolSiC™ MOSFET 1200V M1H offers a new gate source voltage specification in the data sheets for highest flexibility:
  - New recommended gate source voltage window from 15 V to 18 V and from 0 V to - 5 V.
  - The maximum rated gate source voltages (V_{GS}) are extended to 23 V and -10 V to cover over- and undershoots.
- Maximum virtual junction temperature:
  The CoolSiC™ MOSFET 1200V M1H allows operation at a temperature of $T_{vj\,op}$ = 175°C under overload conditions.
- Enhanced stability:
  The 1200 V CoolSiC™ MOSFET M1H offers a new level of threshold voltage stability under real application conditions.

2 Gate-source voltage – the right choice

The CoolSiC™ MOSFET technology is used in a wide range of applications, which by their nature have different and individual needs. The newly introduced CoolSiC™ MOSFET M1H technology offers a flexible gate-source voltage range to simplify the design-in process and to reach the highest utilization levels of the technology in the respective applications.

There are many trade-offs to be considered for choosing the right gate source voltage. The criteria below show an overview about some of the most important parameters that are affected by the choice of gate-source voltage:

- Performance:
  - On-state resistance $R_{DS(on)}$
  - Body diode I-V characteristics
  - Dynamic switching behavior
- Driver stage:
  - Gate charge: driver-output power rating
  - Complexity of the driver stage: unipolar vs. bipolar power supply
- Parasitic turn-on
- $V_{GS(th)}$ drift
- FIT rates
- Short-circuit capability

This chapter explains the impact of the gate-source voltage on the individual parameters listed above.
The data in this chapter was acquired using the 1200 V 53 mΩ Easy 1B device, and is valid for the part number FS55MR12W1M1H_B11. The general behavior can be transferred to other packages or chips using the CoolSiC™ MOSFET M1H technology.

The current CoolSiC™ MOSFET M1H product range of modules is shown in Figure 1.

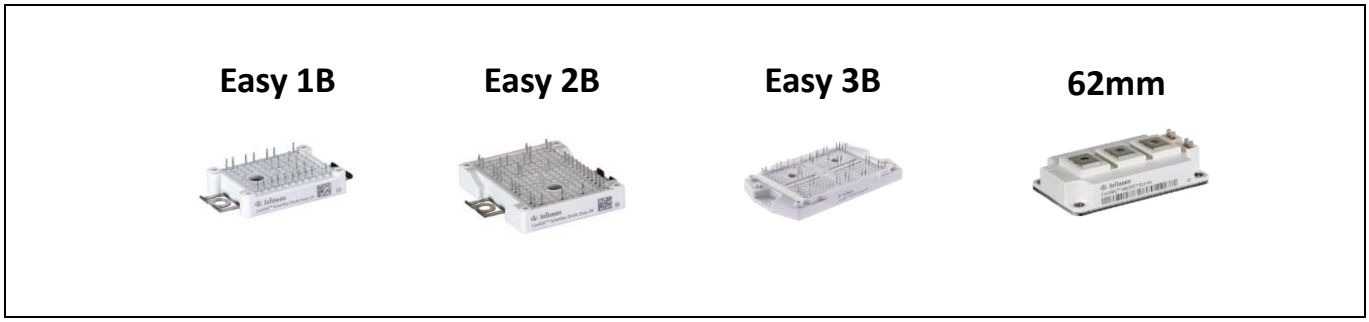

Figure 1 Module solutions using CoolSiC™ MOSFET

2.1 Data sheet definitions of gate-source voltage

One of the advantages of the CoolSiC™ MOSFET M1H technology is that the devices can be operated within a flexible gate-source voltage range. The wide gate-drive voltage window for the positive and negative voltage provides flexibility for the application so that depending on the individual use case the best operation point can be chosen.

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}		T_{vj} = 25 °C	1200	V
Implemented drain current	I_{DN}			15	A
Continuous DC drain current	I_{DDC}	T_{vj} = 175 °C, V_{GS} = 18 V	T_H = 105 °C	15	A
Repetitive peak drain current	I_{DRM}	verified by design, t_p limited by T_{vjmax}		30	A
Gate-source voltage, max. transient voltage	V_{GS}	*D*<0.01		-10/23	V
Gate-source voltage, max. static voltage	V_{GS}			-7/20	V

Table 4 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
On-state gate voltage	$V_{GS(on)}$		15 ... 18	V
Off-state gate voltage	$V_{GS(off)}$		0 ... -5	V

Figure 2 Data sheet values for the gate-source voltages

With regard to the gate-source voltage, we must distinguish between maximum static gate-source voltages, maximum dynamic gate-source voltages and recommended on-state and off-state gate voltages.

The maximum static gate-source voltages describe the steady-stade condition. Gate-source voltages up to +20 V and -7 V set the upper and lower limit. Since this rating is specified as a maximum rated value, it must not be exceeded except for the dynamic condition as described below.

The maximum dynamic gate-source voltages describe the transient voltage peak during the turn-on and turn-off event. It can reach maximum peak voltages of +23 V and -10 V for a duty cycle of less than 1%. Since this rating is specified as a maximum rated value, it must not be exceeded.
The duty cycle is defined as the entire time period as well as the time when the gate-source voltage exceeds the maximum static gate-source voltages. Figure 3 depicts an exemplary gate-source voltage waveform. For simplicity, the envelope (green dotted line in Figure 3) can be used to extract the timeframe t1 and t2. Equation [1] shows how to calculate the duty cycle.

$$D = \frac{t1}{T} = < 1\%; \qquad D = \frac{t2}{T} = < 1\% \qquad [1]$$

In addition to the maximum rated values, Infineon recommends users to drive the devices in a certain voltage range. The on-state voltage range is between + 15 V…+ 18 V and an off-state gate voltage range is between 0…-5 V.
Depending on the individual requirements in the respective application, the $V_{GS(on)}$ and $V_{GS(off)}$ level needs to be defined carefully.

Gate-source voltage – the right choice

The characteristic values in the data sheet of the CoolSiC™ MOSFET M1H are specified at $V_{GS(on)}$ = + 18 V and $V_{GS(off)}$ = - 3 V, which show a good trade-off between performance and lifetime for many applications.

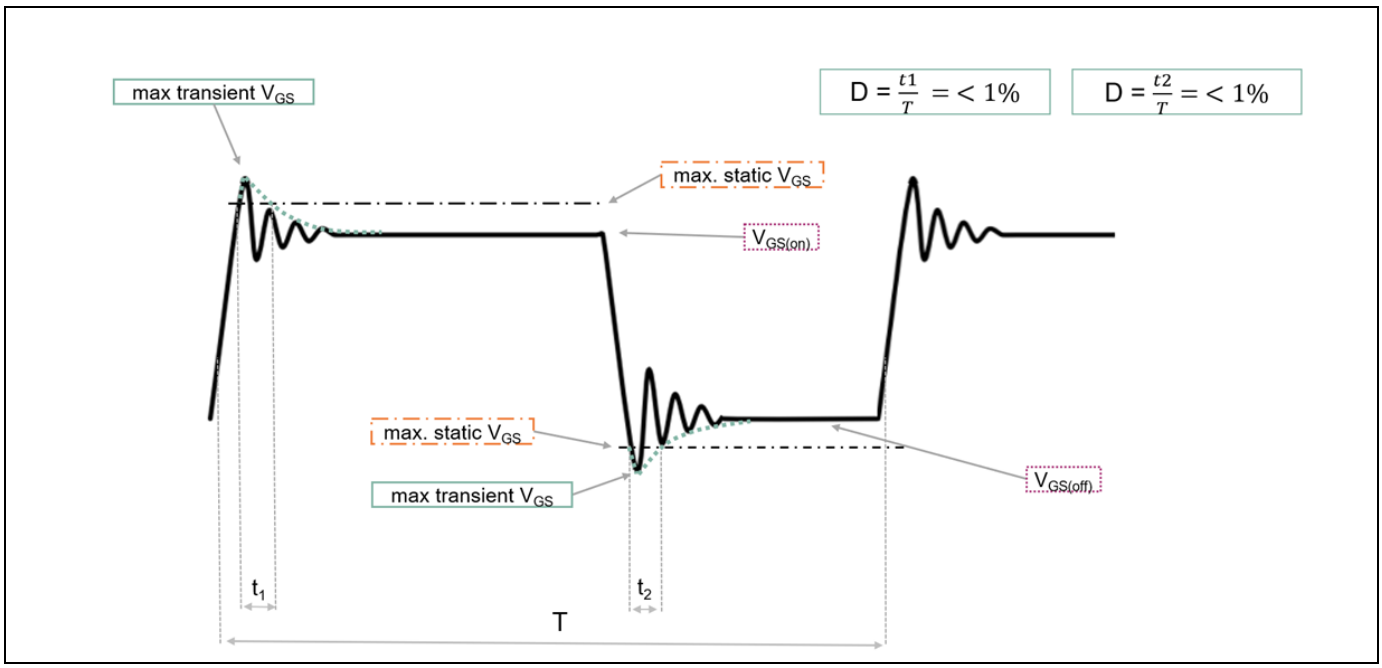

Figure 3 Schematic gate-source voltage waveform

2.2 Device characteristics of CoolSiC™ MOSFET M1H to be considered for the right choice of gate voltage

This chapter describes the impact of the gate-source voltage on several key parameters of the CoolSiC™ MOSFET M1H.

2.2.1 On-state resistance $R_{DS(on)}$

As described in the previous chapter, it is recommended to drive the devices with on-state between +15 V...+18 V and off-state between 0 V…-5 V. Transient peak voltages during the switching event can reach up to +23 V and -10 V with a duty cycle of 1%. Thus the typical on-resistance of the device is determined at $V_{GS(on)}$=+18 V and +15 V in the respective data sheets.

The choice of the on-state gate voltage has an impact on the static performance of the device. The $R_{DS(on)}$ at room temperature as well as the temperature dependency differs amongst different on-state gate voltages.

The I-V curves, or output characteristics, of the MOSFET are measured in pulse mode for different junction temperatures of 25°C, 125°C and 175°C, respectively. Figure 4 (left and right) shows the drain current as a function of drain-source voltage V_{DS} with different on-state gate-source voltages $V_{GS(on)}$. The solid black curves are typical results at 25°C, and the dashed curves are those at higher junction temperature of 125°C and 175°C.

The total $R_{DS(on)}$ resistance is determined by the sum of the single resistances. These are namely the channel resistance (R_{ch}), the resistance of the junction field-effect transistor (R_{JFET}), the epitaxial layer resistance of the drift region (R_{epi}) and the resistance of the highly doped SiC substrate (R_{Sub}). The MOSFET's channel resistance has a negative temperature characteristic due to the behavior of the interface states, while the drift region and intrinsic JFET have positive temperature characteristics. Because of the advantageous channel orientation along the preferred crystal plane with a low density of interface defects, the total $R_{DS(on)}$ of CoolSiC™ MOSFET is not dominated by the MOSFET's channel resistance, so that the total $R_{DS(on)}$ exhibits a positive temperature coefficient in the complete temperature range. This behavior is beneficial for balancing the current distribution

of parallel devices. [1]
Especially the MOSFET channel resistance depends on the applied positive on-state gate voltage. The higher the on-state gate voltage the lower the $R_{DS(on)}$.

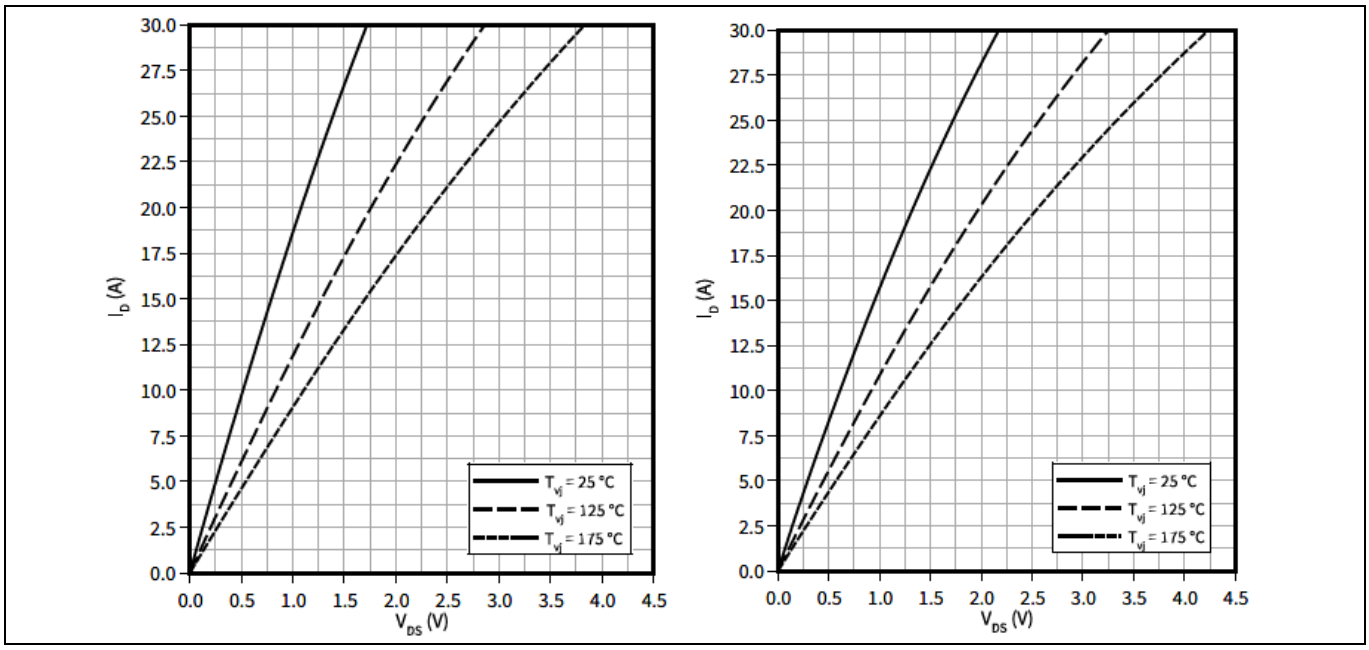

Figure 4 (Left) Typical output characteristics, V_{GS} = 18 V parameter, with T_j=25°C, 125°C and 175°C; (Right) Typical output characteristics, V_{GS} = 15 V parameter, with T_j=25°C, 125°C and 175°C

The on-state resistance $R_{DS(on)}$ as a function of junction temperature T_{vj} is shown in Figure 5 (left). At a rated current of I_{DS}=15 A it amounts to $R_{DS(on)}$=53 mΩ at T_j=25°C, $V_{GS(on)}$ =+18 V and $R_{DS(on)}$=63.5 mΩ at T_j=25°C, $V_{GS(on)}$ =+15 V.
It can be observed that the temperature dependacy for $V_{GS(on)}$ = +18 V is more pronounced than for $V_{GS(on)}$ =+15 V. This effect is a consequence of less contribution of the MOSFET channel resistance and a more dominating epitaxial layer resistance at different on-state gate voltages. [1]

As the SiC MOSFET is a voltage-controlled device, it turns on gradually with increasing gate-source voltage. The right curves of Figure 5 are almost linear up to drain currents of about 30 A, if the gate source voltage is above 13 V. For higher drain currents or lower gate-source voltages, there is a significant reduction of the current slope with increasing V_{DS}. This behavior is a consequence of the built-in junction field effect transistor (JFET), which is formed by the deep p+ wells. As the p+ wells are linked to source, the junction channel of the JFET is controlled by a drain-source voltage drop. Hence, the JFET channel is narrowed down with increasing V_{DS}. [1]

Exceeding 13 V of gate voltage, the drain current decreases with temperature, resulting in better paralleling performance of multiple devices. Below 13 V gate voltage, the drain current increases with temperature. It is not recommended to have $V_{GS(on)}$ below +13 V for on-state.

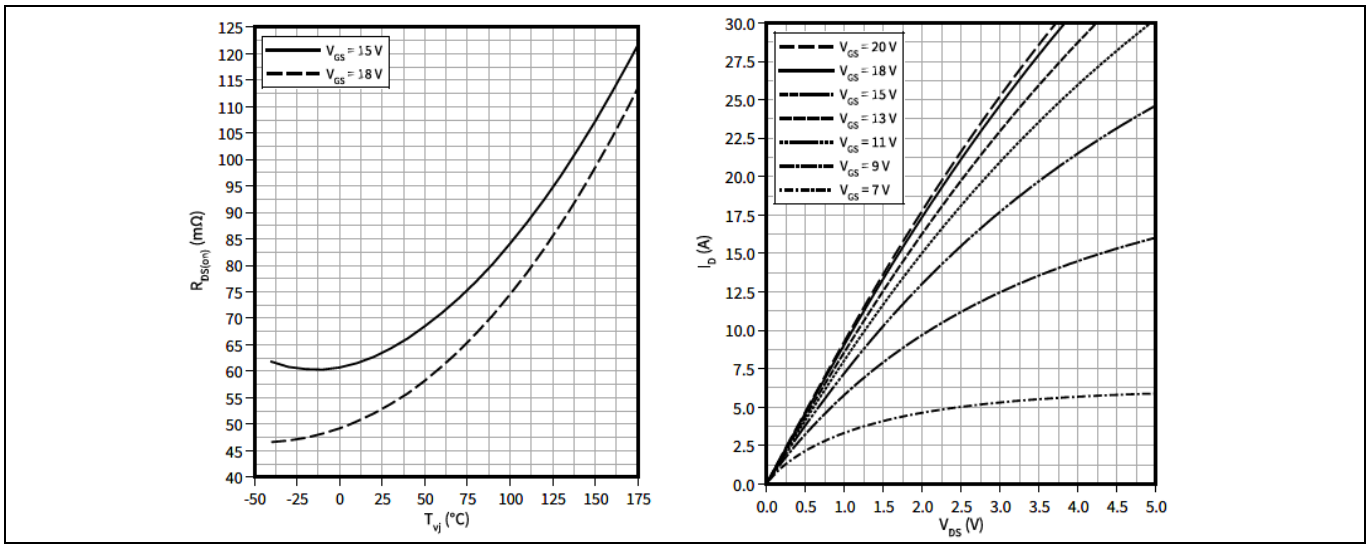

Figure 5 (Left) Typical on-resistance vs. junction temperature. I_{DS} = 15 A, V_{GS} = 18 V & 15 V; (Right) Typical output characteristics, V_{GS} = +7..+20 V parameter, with T_j = 175°C

2.2.2 Forward characteristics of the body diode

The choice of the off-state gate voltage also has an impact on the performance of the body diode.
The CoolSiC™ MOSFET M1H integrates an intrinsic body diode with p-n junction behavior. As shown in Figure 6 (left), the intrinsic bipolar body diode has a relatively high forward voltage V_{SD} (about 4.2 V at 15 A, V_{GS}=-3 V) compared to silicon parts. The forward voltage drop changes with the negative gate voltage. For 0 V the forward voltage is lower than for -5 V.

The forward voltage V_{SD} has a negative temperature coefficient, and the temperature dependency is almost similar for gate voltages between 0 V and -5 V (see Figure 6 on right).

Since the voltage drop is quite high, it is not effective to use the body diode to conduct current for long periods of time. Fortunately, the CoolSiC™ MOSFET M1H can conduct reverse current from source to drain through the channel if a positive bias is applied to the gate. This mode of operation is called synchronous rectification (or third quadrant operation) and achieved by a positive on-state gate voltage of typically +15 V…+18 V on the gate. As shown in Figure 6 (left), synchronous rectification mode is highly recommended to limit conduction losses. Similar to the forward direction of the MOSFET, +18 V shows lower V_f than +15 V.

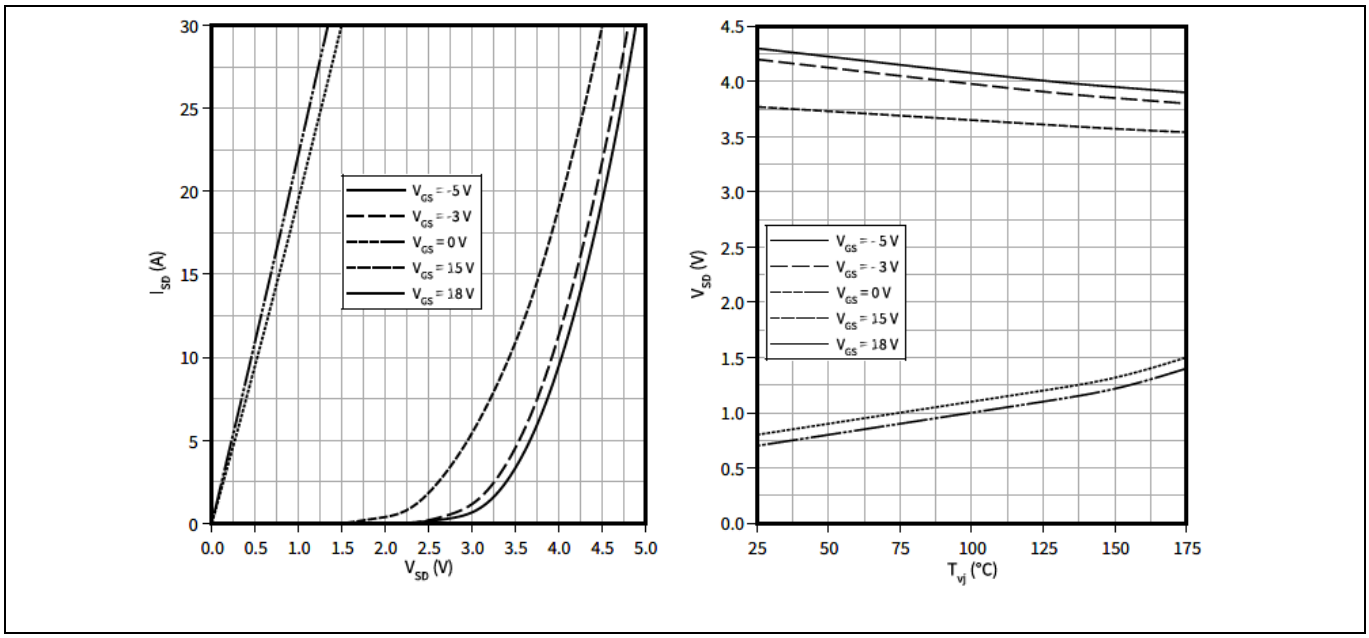

Figure 6 **(Left) Reverse current I_{SD} as function of voltage at different gate voltages and T_{vj} =25°C (Right) V_{SD} temperature dependency at different gate voltages**

Applying synchronous rectification has the additional benefit that positive temperature coefficient of the MOSFET in reverse direction will support current sharing in case of paralleling. Figure 7 shows exemplary waveforms for four modules in parallel. The first pulse is making use of synchronous rectification after the dead time, while for the second pulse the the body diode is conducting the current. The results confirm that synchronous rectification leads to a better current sharing between the current waveforms.

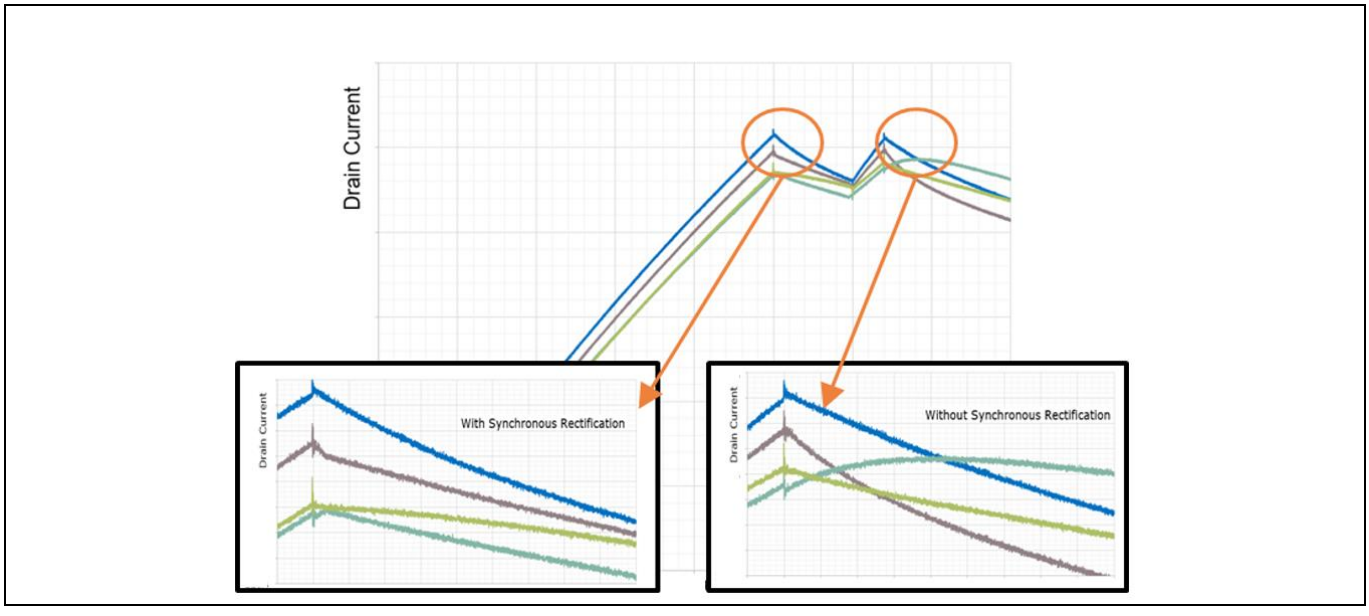

Figure 7 **Paralleling of four modules: drain current waveform with and without synchronious rectification**

2.2.3 Dynamic behavior

During every switching event, the effect of the $V_{GS(th)}$ hysteresis can be observed. This effect is best visible by measuring the gate charge, the transconductance, or by comparing the switching waveforms for turn-on and turn-off. The lower the level of $V_{GS(off)}$, the better the hysteresis effect can be observed.
A turn-on from $V_{GS(off)}$ = -5 V would lead to a dynamically reduced threshold voltage compared to a turn-on from

Gate-source voltage – the right choice

$V_{GS(off)}$ = -0 V. At -5 V, an earlier start of the Miller phase can be observed, and the voltage during the Miller phase is lower which results in a higher transconductance [3]

Where a constant delta between $V_{GS(off)}$ & $V_{GS(on)}$ was applied, e.g -5 V/+15 V & -2 V/+18 V, investigations showed that the Miller phase was reached earliest at the lowest $V_{GS(off)}$ level, resulting in the highest transconductance [3].

In case the $V_{GS(on)}$ is kept constant, e.g at 18 V, the lowest $V_{GS(off)}$ level shows the highest dv/dt during turn-on. Figure 8 (left) shows the maximum dv/dt during turn-on for different $V_{GS(off)}$ levels and a constant $V_{GS(on)}$ of 18 V. However, for turn-off, the Miller ramp is independent of the $V_{GS(off)}$ level at the same position. Nevertheless, a slight acceleration can be observed, but mainly due to higher driving voltage, e.g 0 V/+18 V vs. -5 V/+18 V (see Figure 8 (right)) [4].

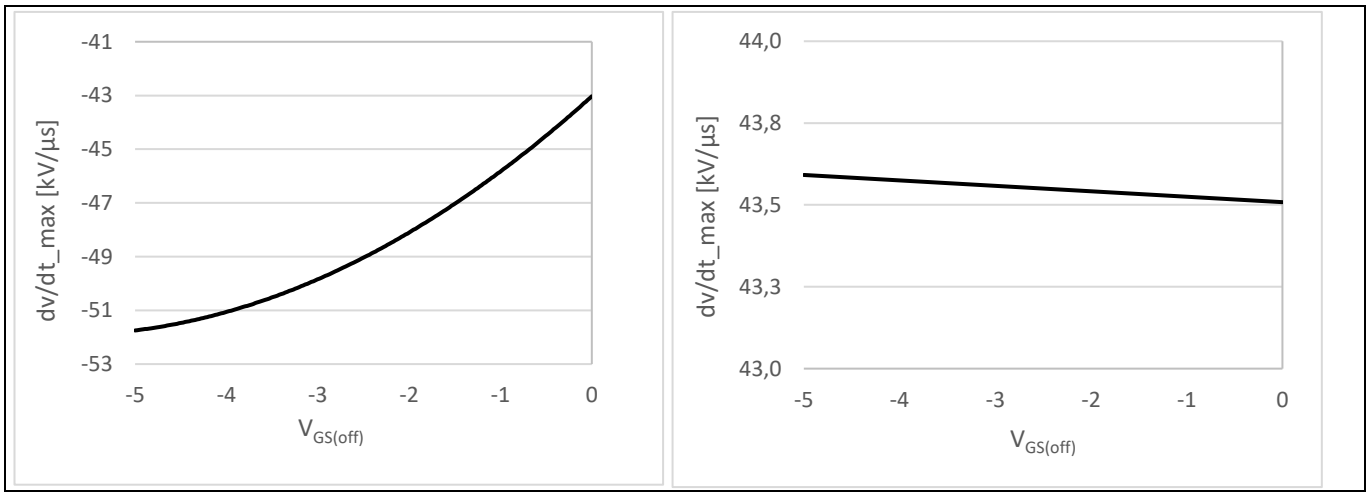

Figure 8 **(Left) Turn-on with FS55MR12W1M1H_B11: dv/dt vs. $V_{GS(off)}$ @ DC-link=600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff} = 3 Ω, I_{DS} = 15 A, V_{GS} = 18 V.**
(Right) Turn-off with FS55MR12W1M1H_B11: dv/dt vs. $V_{GS(off)}$ @ DC-link=600 V, T_{vjop} = 25°C, R_{gon}= 4 Ω, R_{goff} = 3 Ω, I_{DS} = 15 A, V_{GS} = 18 V.

2.2.4 Parasitic turn-on

Many applications that make use of the CoolSiC™ MOSFET modules try to minimize switching loss accepting steep transients in voltage and current. Therefore, the immunity of the device against parasitic turn-on is paramount. With the CoolSiC™ MOSFET M1H, this topic has been addressed in the chip design.

Unwanted parasitic turn-on of a semiconductor switch can occur when its antiparallel diode is turned off. A schematic scenario is shown in the drawing in Figure 9. The current I_L is freewheeling via the body diode of the low-side device S2 until switch S1 turns on. When the load current has fully commutated to S1, S2 starts to block a voltage between the drain and source. Via the Miller capacitance C_{GD}, the rising drain potential on S2 pulls up the gate voltage. In case the threshold level is exceeded a shoot-through occurs [2].

Gate-source voltage – the right choice

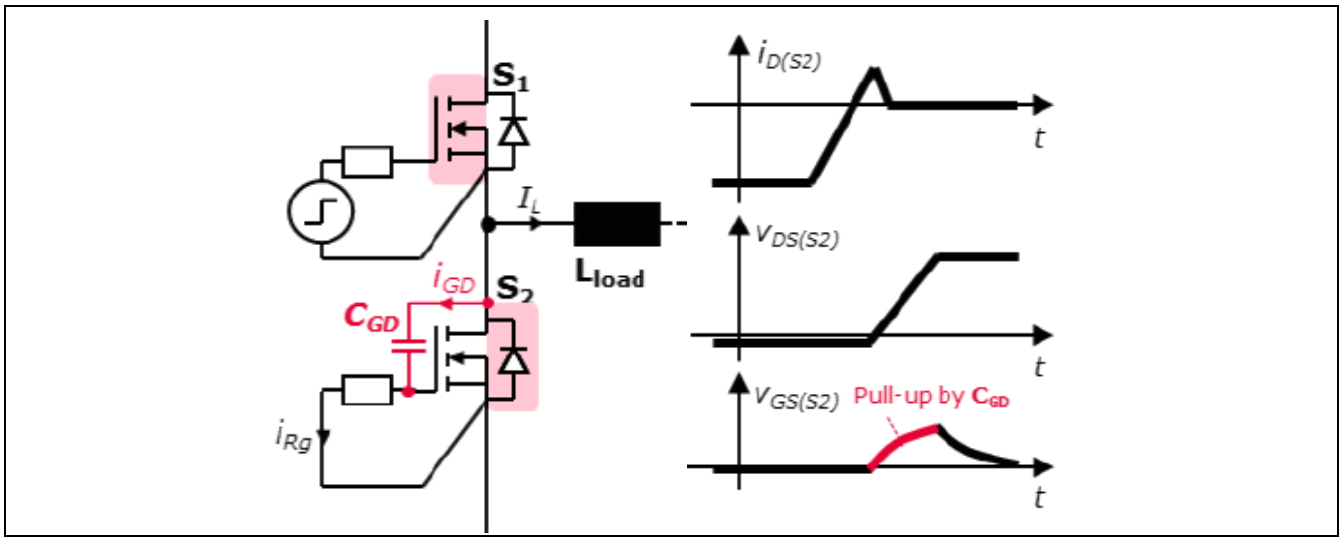

Figure 9 Schematic explaination for a parasitic turn-on event [2]

The gate-charge characteristic of a certain device gives an indication of the principal resilience against parasitic turn-on. The lower the ratio $Q_{GD}/Q_{GS,th}$ of a device the higher the resilience. Devices with a charge ratio smaller than one are considered insusceptible to parasitic turn-on as far as inductive voltage drops can be neglected. That holds true for CoolSiC™ MOSFET M1H technology. While a brief look at the data sheet of a certain switch is enough to get an impression of the charge ratio and susceptibility to parasitic turn-on, the indication is often rather qualitative. First, the influence of the blocking voltage is typically not shown, and second, due to the DIBL effect (drain-induced barrier lowering), a clear separation of $Q_{GS,th}$ and Q_{GD} is difficult [2].

Another indication in regard to the immunity against parasitic turn-on is given by the threshold voltage $V_{GS(th)}$. The threshold voltage is the gate-source voltage needed for current to start flowing through the channel of the device at a specific drain-to-source current. Figure 10 (left) shows the threshold voltage versus temperature at I_{DS} = 6 mA for the 53 mΩ device. The threshold voltage $V_{GS(th)}$ is measured by first applying one 1 ms pulse-gate voltage at a V_{GS} = +20 V as a precondition [1, 6], then the threshold-voltage value of $V_{GS(th)}$ is read at V_{GS}= V_{DS} by forcing current I_{DS} = 6 mA . From the results, the typical threshold voltage $V_{GS(th)}$ equals 4.3 V at 25°C and I_{DS}= 6 mA, which provides good noise immunity against parasitic turn-on, meaning ease of use for the device.

Typically, SiC MOSFETs have a short-channel effect resulting in a reduction of threshold voltage at higher drain voltages. The effect is called DIBL already known from low-voltage Si power MOSFETs. [1]. For the CoolSiC™ MOSFET M1H, the $V_{GS(th)}$ is reduced when blocking V_{DS} voltage increases as shown in Figure 10 on the right. With DC voltage at normal maximum operating voltage of 800 V, the $V_{GS(th)}$ of CoolSiC™ MOSFET M1H is typically 2.6 V at a junction temperature of 150°C.

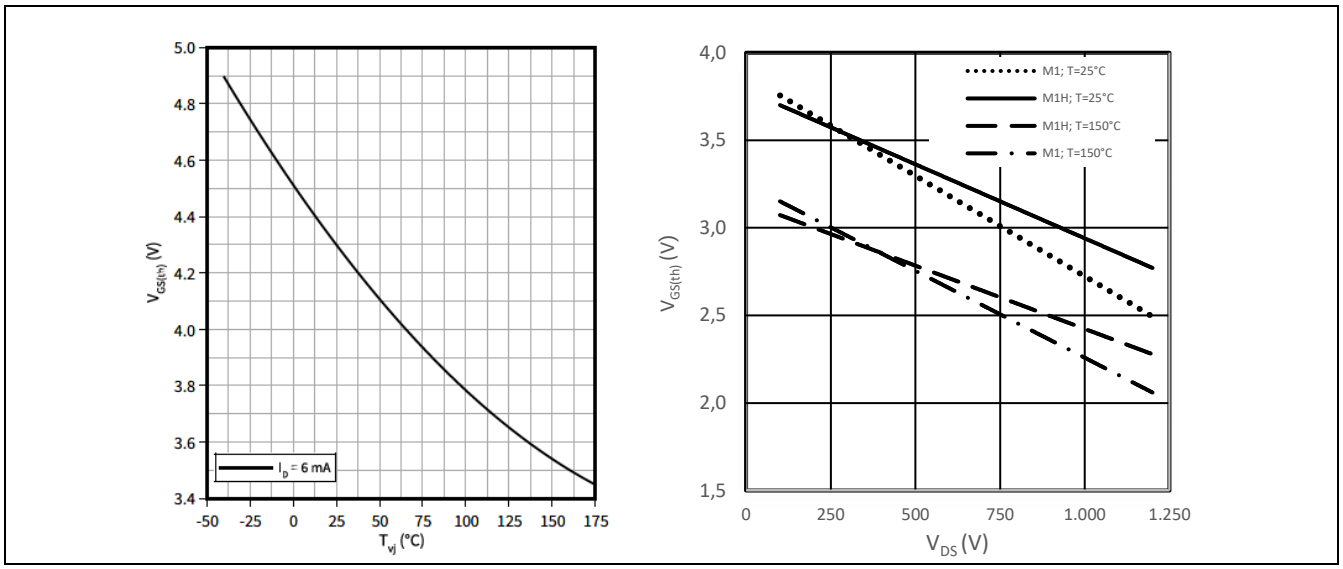

Figure 10 (left) Typical gate-source threshold voltage as a function of junction temperature (I_{DS}=6 mA, V_{GS}=V_{DS}); (right) Typical gate-source threshold voltage as a function of drain-source voltage ($T_{vj,op}$ = 150°C)

If a parasitic turn-on occurs, additional losses can be observed. Figure 11 shows the turn-on losses of the FS55MR12W1M1H_B11 for different $V_{GS(off)}$ levels. For the measurements a double pulse test setup was used, where the active switch is turned off with -3 V, while the negative gate-sourve voltage of the passive switched was varied between 0… -5 V. The turn-on losses of the active switch start slightly to rise from -2 V for the passive switch, which indicates that a parasitic turn-on occured.

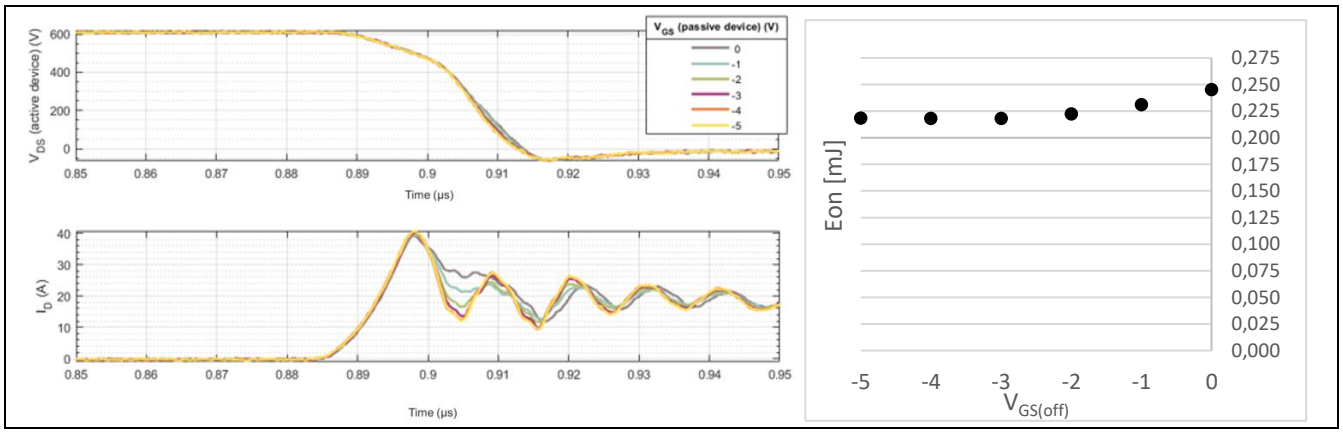

Figure 11 (left) FS55MR12W1M1H_B11: Turn-on @ DC-link=600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff} = 3 Ω, I_D=15 A. Passive switch $V_{GS(off)}$ = 0…-5 V; Active switch at $V_{GS(off)}$ = -3 V
(right) FS55MR12W1M1H_B11: Eon (active switch) vs. $V_{GS(off)}$ (passive switch) @ DC-link = 600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff} = 3 Ω, I_D=15 A; Active switch at $V_{GS(off)}$ = -3 V

The following parameters have an impact:

- Temperature – $T_{vj\,op}$
- DC-link voltage - V_{DS}
- R_{gon} of the active device and R_{goff} of the passive device
- Gate-source voltage - $V_{GS(on)}$ & $V_{GS(off)}$
- Current - I_D

Gate-source voltage – the right choice

Depending on the individual requirements in the respective application, the $V_{GS(off)}$ level needs to be defined carefully in order to prevent parasitic turn-on or to keep the additional losses at an acceptable level.

2.2.5 Dynamic characteristics of the passive switch

The SiC-MOSFET die operated in the freewheeling path (S2 in Figure 9) contains two internal structures, the MOSFET with gate and channel as well as bipolar diode structure, usually referred to as body diode. Both structures contribute to the dynamic behaviour as follows;

- Capacitive contribution from both parts, leading to a capacitive charge Q_C and a stored energy E_{oss}
- Contribution from the plasma in the bipolar diode, negligible at moderate currents and temperatures but becoming relevant at more demanding conditions
- Contribution from the SiC-MOSFET due to parasitic turn-on

When performing a measurement of E_{fr} according to IEC 60747-8, which is comparable to measuring reverse recovery of a diode, this measurement will only show the summed up effect of all three contributions. However the dependencies and the thermal effects will be different.

- For the capacitive contribution there is no other significant parameter relevant beside the DC-link voltage. The energy E_{oss} will be dissipated at the next turn-on event of this device in case of hard switching or is recovered in case of soft switching
- The contribution from plasma, beside parameters already mentioned, a function of di/dt and stray inductance. As the off-state voltage also governs current sharing between channel and diode structure this has to be considered as a furher parameter. This energy has to be considered as switching loss
- The contribution from parasitic turn-on varies with the gate condition on the passive switch and the duration the diode as been in conduction mode. Figure 11 describes the impact of the gate driving condition on the passive switch. Details on the impact of conduction time are provided in [7]. Also this energy contributes to switching loss.

The datasheet only documents the overall value of charge and energy to keep data simple and transparent. As these losses usually are small in relation to E_{on} and E_{off} this is regarded as acceptable.

2.2.6 Gate charge and gate driver output power rating

The total gate charge Q_G is defined as the charge from the origin (e.g. $V_{GS(off)}$ = - 3 V) to the point on the curve at which the driving voltage equals the actual gate-to-source voltage of the device (e.g. $V_{GS(on)}$ = 18 V). Thus the choice of the on-state and off-state gate voltage has an impact on the share of gate charge needed when using a lower voltage range for driving. Figure 12 provides the gate-charge characteristic at I_{DS}=15 A for the FS55MR12W1M1H_B11. Here the typical value of Q_G=0.045 µC can be read off. This means that depending on the applied gate-source voltage, the required gate driver output power (P_{GD}) can be derived accordingly.

$P_{GD} = f_{sw} \times Q'_G \times \Delta V_{GS}$

f_{sw} = SiC MOSFET switching frequency

Q'_G = Gate charge, reading taken from diagram for the voltage range actually used

$\Delta V_{GS} = |V_{GS(on)}| + |V_{GS(off)}|$ (Steady state values)

As explained in Chapter 2.2.3, the start of the Miller ramp depends on the applied negative gate-source voltage.

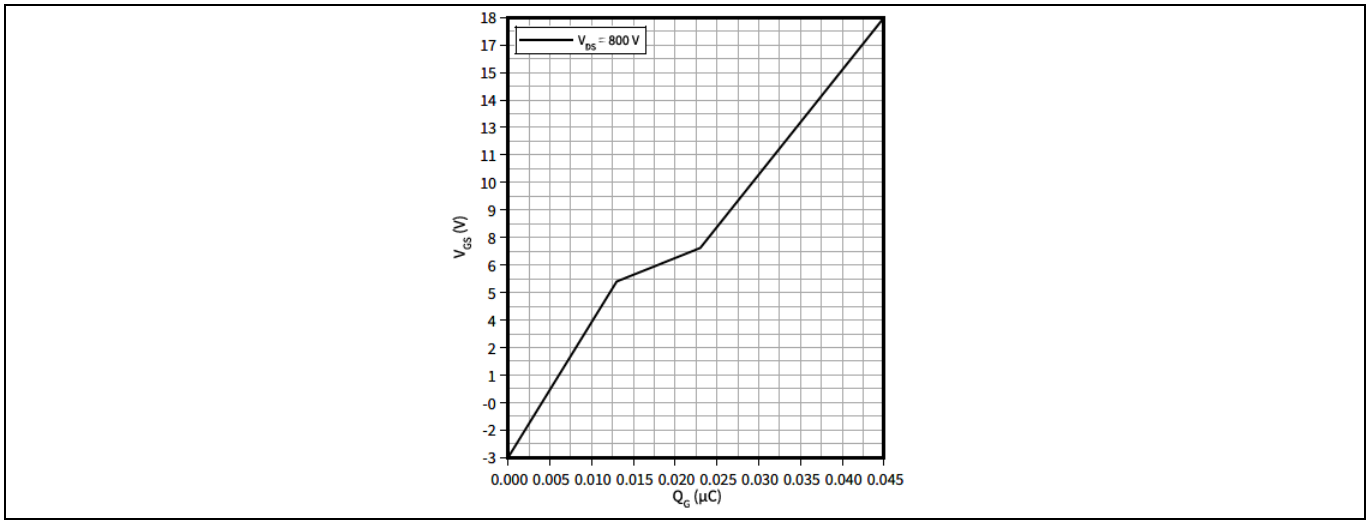

Figure 12 Typical gate charge, $V_{GS} = f(Q_G)$, $I_{DS} = 15$ A, $V_{DS} = 800$ V, turn-on pulse

2.2.7 Short-circuit capability

Figure 13 depicts typical short-circuit waveforms for different $V_{GS(off)}$ voltages. Initially, the drain current increases rapidly and reaches the peak current level. After peak current has been reached, the drain current is significantly decreased. This is due to the reduction in carrier mobility and JFET effect with temperature increase as a consequene of self-heating. The waveforms show clean and robust behavior, which proves the typical 2 µs SC capability. Typically, the respective modules can withstand 10 short-circuit events over lifetime.

The peak current level at the beginning strongly depends on the DC-link voltage, the temperature, the module internal layout concept and the applied $V_{GS(on)}$ and $V_{GS(off)}$ level.
Due to the DIBL effect with increasing DC-link voltage or temperature, the saturation current rises more strongly [4].
The same holds true for the applied $V_{GS(off)}$ level. The lower the applied $V_{GS(off)}$ voltage, the higher is the peak current when the short circuit starts to occur. Figure 13 shows clearly that the peak current is higher for $V_{GS(off)}$ = -5 V than for $V_{GS(off)}$ = 0 V. This effect needs to be considered for the short-circuit protection design.
Depending on the module's internal layout concept, current rises slower when a negative feedback is induced via the di/dt against the applied V_{GS}. In such cases the peak current is reduced, but dynamic losses are higher.

Please note:
Not all modules are specified with short-circuit capability in the respective data sheet. In cases where a short circuit is specified, it is mandatory to apply +15 V for $V_{GS(on)}$ and 0…-5 V for $V_{GS(off)}$ for the above-mentioned reasons.

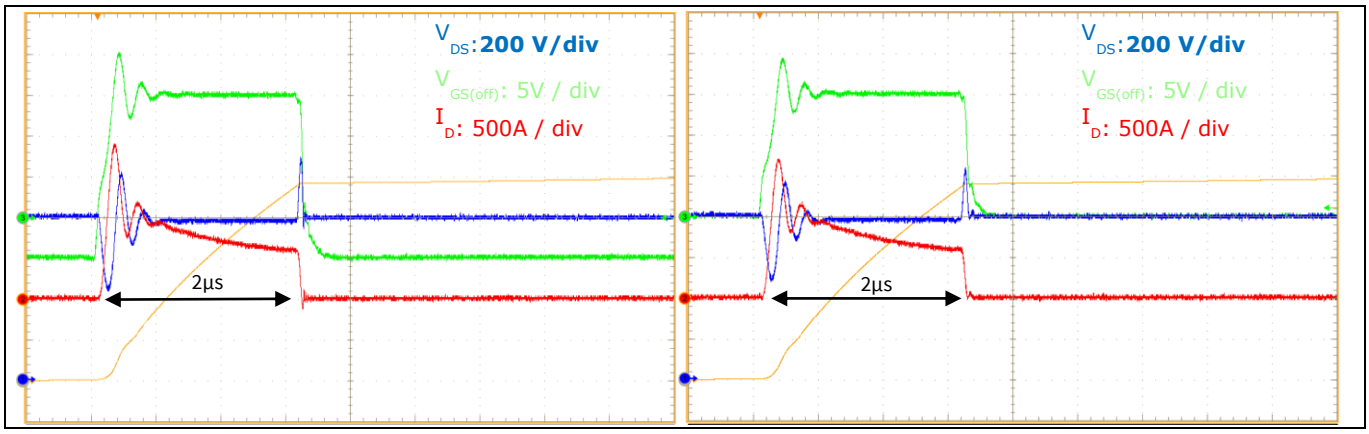

Figure 13 (left) Typical short-circuit waveforms at VDS = 800 V and VGS = -5 V (right) Typical short-circuit waveforms at VDS = 800 V and VGS = 0 V

2.2.8 $V_{GS(th)}$-Drift

The 1200 V CoolSiC™ MOSFET M1H shows significant improvements with regard to threshold voltage stability. This allows designers to significantly extend the allowed gate operation window in comparion to 1200 V M1. Extensive tests under various operation conditions were carried out by Infineon to develop a predictive model that describes the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}). This gives the opportunity to accurately predict the worst-case $R_{DS(on)}$ change for arbitrary mission profiles.

To assess the worst-case, end-of-mission profile (EoMP) $R_{DS(on)}$ drift for individual applications, one needs to consider the total number of switching events until EoMP. This number can be easily calculated from the lifetime target, the total operation time and the switching frequency of the application. With the number of switching cycles (N_{cycles}) the relative change in $R_{DS(on)}$ can be extracted from Figure 14.

Please note:

Figure 14 considers the maximum positive and negative dynamic gate-source voltage of the respective data sheets. Both diagrams represent drift values under worst-case conditions, and are valid as long as the devices do not exceed the data sheet limits of the respective product. The diagrams enable the customers to choose any parameter set inside the data sheet framework that fits their application best, without spending much effort on considering the drift impact and parasitic over- & undershoots in the gate signal.

Applications running at well-controlled gate-bias levels that are well below the data sheet maximum limits may exhibit even lower $R_{DS(on)}$ drift values for the same number of switching cycles, as shown in Figure 14 [3].

When operating at a less negative turn-off gate voltage (e.g. -2 V instead of -5 V), the impact on the application is slight. Several application-relevant parameters should be considered, e.g. E_{on} and E_{off} will change slightly and the forward voltage of the SiC MOSFET body diode will be reduced.

Gate-source voltage – the right choice

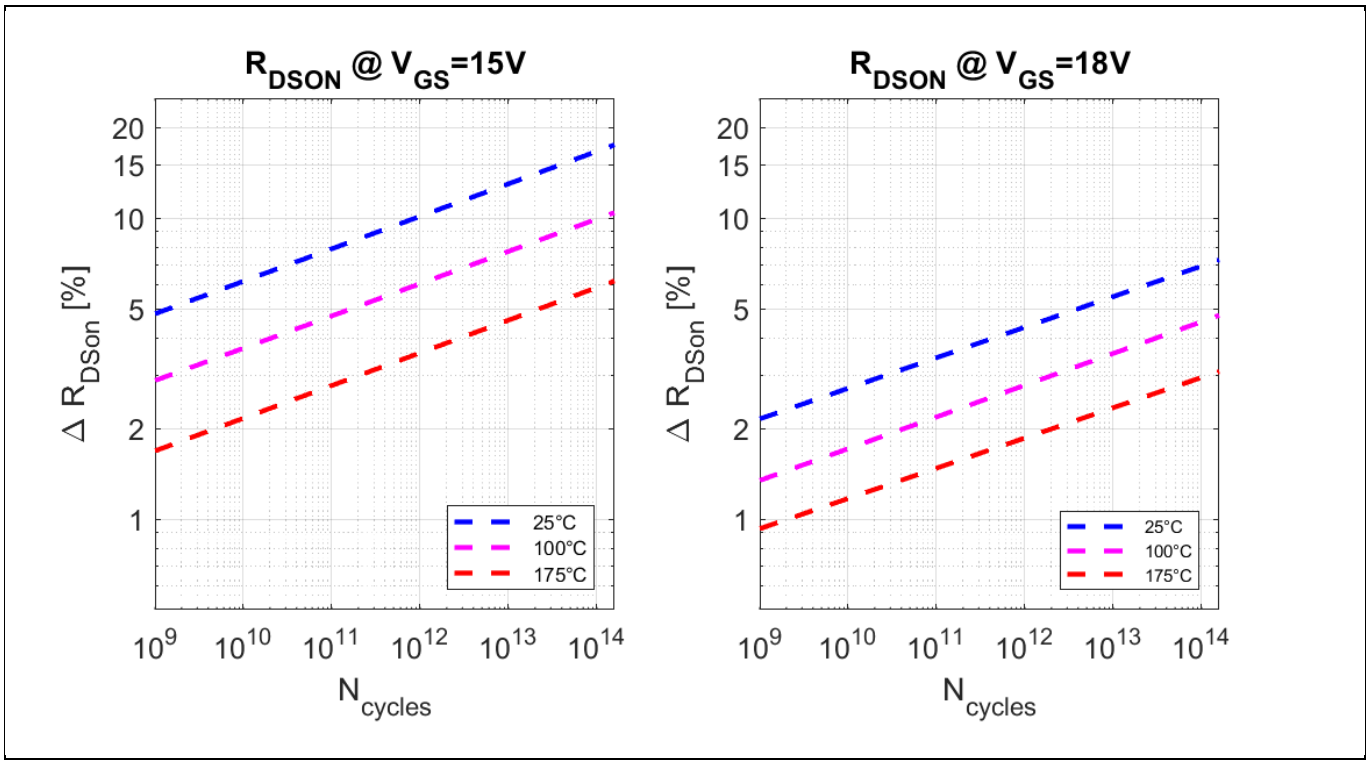

Figure 14 (left) Relative $R_{DS\,(on)}$ change @ $V_{GS(on)}$ = 15 V, T_{vjop}=25°C,125°C & 175°C; (right) relative $R_{DS(on)}$ change @ $V_{GS(on)}$ = 18 V, T_{vjop}=25°C,125°C & 175°C

How to use this information is explained in the following example:

Targeted lifetime: 20 years

Real operation time: 50 % = 10 years

Real operation time: 315360000 s (10 years)

Switching frequency: 48 kHz

Cycle duration: 1 / switching frequency = 0.0000208 s

Number of cycles at end of life: operating time / cycle duration = ~1.52E+13

For a turn-on voltage of 18 V, an $R_{DS(on)}$ change of ~6% @ 25°C and ~3% @ 175°C can be expected, as shown in Figure 14 on the right.

For a turn-on voltage of 15 V, a change in $R_{DS(on)}$ of ~13% (25°C) and ~5% (175°C) can be predicted (see Figure 14 on left).

For more information please see: AN2018-09 Guidelines for CoolSiC MOSFET gate drive voltage window

2.2.9 FIT rates and lifetime

To describe FIT rates the bathtub curve is widely used. The bathtub curve can be divided into three parts.
A first part with a decreasing failre rate, also known as early failure. Screening processes in the production lines have the task to sort out weak devices to exclude them from the field.
The second part shows a constant flat failure rate. For SiC MOSFETs this area is mainly defined by gate oxide fails and cosmic ray effects.
In the last and third part an increasing failure rate can be observed. This section is also known as wearout (intrinsic material failures).

For on-state operation, Infineon recommends V_{GS} = +15 V…+18 V of its CoolSiC™ and for off-state operation V_{GS} = 0 V…-5 V of its CoolSiC™ MOSFET M1H. The trade-off between long lifetime and performance is well-balanced for this operation voltage.
In general, our device could be driven with higher gate-source voltages than 18 V, which further improves the on-state behavior. However, the lifetime of the gate oxide will be reduced, since gate-oxide stress is higher, thus accelerating the aging of the device. Furthermore, the failure rate is increased by using a higher gate-source voltage than 18 V.

For operating conditions, deviating from Infineons recommendations, please check with Infineon about the impact on lifetime and FIT rates.

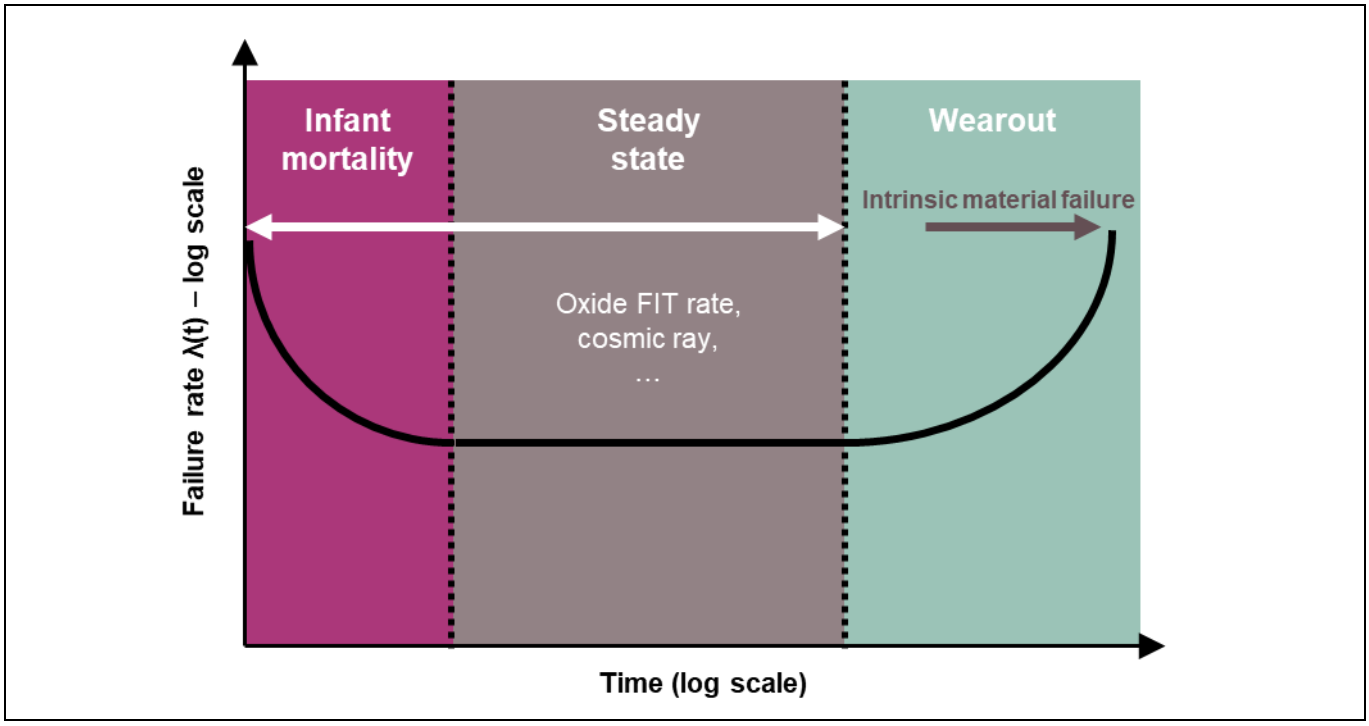

Figure 15 Typical bathtub curve

3 Maximum virtual junction temperature $T_{vj\ op}$

3.1 Definition of 175°C operation junction temperature

The CoolSiC™ MOSFET 1200V M1H allows operation at a temperature of $T_{vj\ op}$ = 175°C under overload conditions. This matches the typical requirement in several application where high current and thus temperature is only required in the short term.

Figure 16 shows the definition of the allowed operation junction temperature under switching conditions for CoolSiC™ MOSFET 1200V M1H. For normal operation, the maximum junction temperature is 150°C. During overload conditions, a maximum junction temperature above T_{vjop}= 150°C and up to T_{vjop} = 175°C is allowed for a maximum duration of t_1= 60 seconds. The overload duration where the T_{vjop} is above 150°C must be within 20% of the load cycle time (T), e.g. t_1=60 s every T=300 s. Using this increased junction temperature capability, compared to a maximum T_{vjop}=150°C, can enable higher power density, but also can result in higher heatsink temperatures.

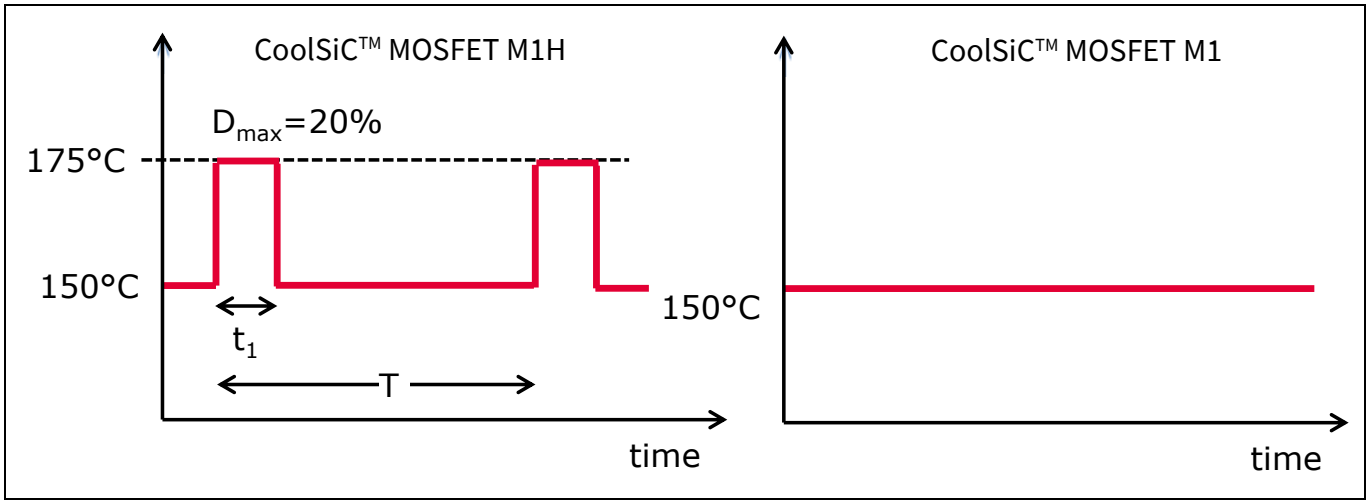

Figure 16 Maximum operation junction temperature definition for CoolSiC™ MOSFET M1H and M1

The maximum temperature definition shown in Figure 16 should be considered as the maximum T_{vjop} limitation including the temperature ripple due to the fundamental output frequency. Figure 17 provides two examples of junction temperature profiles. In Figure 17 (left), T_{vjop} exceeds 150°C for t_1 = 50 s. It is below 150°C for the rest of the T = 300 s cycle. Therefore, the duty cycle is 16.7%. This condition would be allowed from the point of view of a maximum operating junction temperature. Another example is shown in Figure 17 on the right. In this case the temperature exceeds the maximum curve of the junction temperature for the whole period of the load profile. Therefore, this operation would not be allowed.

The number of hours the temperature is allowed to exceed the 150°C in the application depends on the time constant of the heat sink. In addition, excessive operation with this load profile at boundary conditions for more than several hundred hours can lead to traces of silicone oil on the module housing. If this type of load profile is to be used for a high number of hours, please contact your Infineon support channel to perform a detailed analysis regarding this specification.

Maximum virtual junction temperature Tvj op

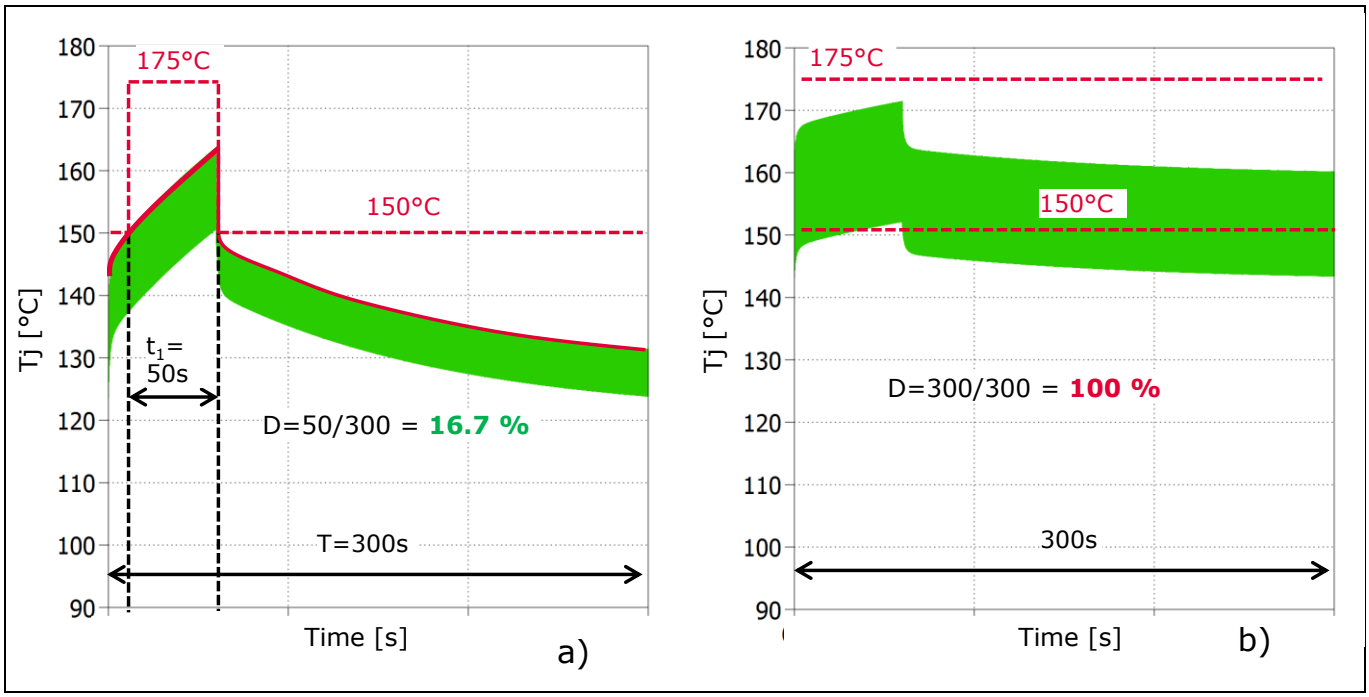

Figure 17 Examples illustrating when the 175°C junction temperature operation is allowed (left) and not allowed (right)

3.1.1 System-temperature limitation for even higher operation temperature

The CoolSiC™ MOSFET M1H allows a 25 K higher operation junction temperature than the M1. With this feature, the system using M1H has even higher power density and component temperatures, e.g. PCB, heatsink and module frame. Several restrictions should be considered as described below.

3.1.1.1 Frame-temperature limitation

The RTI (relative temperature index) value is specified in the datasheet. The value is the characteristic parameter related to thermal degradation of the plastic material. During the operation, the module-frame temperature should not exceed this value. Otherwise, the UL standard ratings will be violated.

3.1.1.2 PCB-temperature limitation

With the increased junction temperature, the power density of the system can be higher. This means that the current that goes through each pin can increase, as some pinouts for M1 and M1H modules are the same. With this increase in current, the PCB temperature rise should be carefully considered. The maximum allowed PCB temperature depends on the PCB material itself. Thicker copper layers, wider tracks, increased number of layers, and system cooling can help to reduce PCB temperature.

3.1.1.3 Heatsink-temperature limitation

The heatsink temperature should not exceed the allowed operation temperature of the thermal interface material if the module is pre-applied with Infineon's thermal interface material TIM.

4 Glossary

$R_{DS(on)}$	Resistance at the actual junction temperature, given at the datasheet current I_{DS}
$V_{GS(th)}$	Voltage between gate and source at which current starts to flow
I_{DSS}	Drain-source leakage current at shorted gate-source voltage = 0 V and V_{DSS}= 1200 V
V_{GS}	Bias between gateand source, corresponds to V_{ge} in an IGBT
I_{DS}	Load current flowing between drain and source
V_{DS}	Bias between drain and source, corresponds to V_{ce} in an IGBT
C_{rss}	This value is defined as defined as the capacitance effective between gate and drain. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the gate-drain capacitance.
C_{gs}	Effective capacitance between source and gate
C_{iss}	This value is defined as the capacitance effective between gate and source. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the sum of gate-source capacitance and gate-drain capacitance.
C_{gd}	Effective capacitance between drain and gate
C_{oss}	This value is defined as the capacitance effective between source and drain. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the sum of gate-drain capacitance and gate-source capacitance.
C_{ds}	Effective capacitance between source and drain
R_{G_int}	Effective internal gate resistance, comprising the sum of the resistance of the distributed gate network and additional resistors added to the gate pad
E_{on}	Turn-on loss energy, measured according to IEC 60747-8
E_{off}	Turn-off loss energy, measured according to IEC 60747-8
E_{tot}	Total loss energy, sum of E_{on} and E_{off}
Q_{GD}	Typically the gate charge needed to pass the Miller plateau
Q_G	Total gate charge
$Q_{GS,pl}$	Gate charge needed to reach the Miller from the off-state V_{GS}
R_G	Externally applied gate resistance, adds to R_{G_int}
$R_{G(on)}$	Externally applied gate resistance for turn-on
$R_{G(off)}$	Externally applied gate resistance for turn-off
$T_{vj\,op}$	Virtual junction temperature during operation. The term “virtual” refers to a temperature measured by temperature sensitive electrical parameters as described in the standards of the IEC 60747 series

5 Reference

[1] AN2017-46: CoolSiC™ 1200 V SiC MOSFET Application Note; July 2018

[2] K. Sobe: Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs; May 2019

[3] AN2018-09: Guidelines for CoolSiC MOSFET gate drive voltage window; March 2022

[4] T. Basler: Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET

[5] AN2018-14: TRENCHSTOP™ 1200 V IGBT7 T7 Application Note; June 2021

[6] FS55MR12W1M1H_B11 data sheet: Revision 1.20, 2022-06-09

[7] Understanding the Turn-off Behavior of SiC MOSFET Body Diodes in Fast Switching Applications; May 2021

Revision history

Document version	Date of release	Description of changes
Revision 1.0	2022-06-09	First release

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